Application Notes: SY8106A

High Efficiency, Fast Response, 6A, 18V Input Synchronous Step Down Regulator with I²C Interface

General Description

SY8106A develops a high efficiency synchronous buck regulator capable of delivering 6A output current. The device operates over a wide input voltage range from 4.5V to 18V. SY8106A adopts instant PWM architecture to achieve fast transient response.

SY8106A integrates an I²C compatible interface for output voltage setting, status read back, etc. The device also features enable control, open drain power good indicator, cycle-by-cycle current limit, short circuit protection and thermal shutdown.

SY8106A provides compact solution for TCON power system. It is available in a QFN3x3-20 package.

Ordering Information

SY8106 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8106ARAC	QFN3x3-20	--

Applications

- TCON Power System
- Mobile handsets
- Portable applications

Features

- 4.5V to 18V input voltage range
- 6A synchronous buck regulator:
  - Low $R_{DS(ON)}$ for internal switches (Top FET/Bottom FET): 50/15 mΩ
  - 6.0A output current capability
  - Instant PWM architecture to achieve fast transient responses
  - 200kHz to 1MHz programmable switching frequency
  - I²C programmable output voltage with initial voltage setting by resistor divider
  - 0.6V+/-1% feedback reference voltage
  - Enable control
  - Power good indicator
  - Adjustable soft-start time
  - PSM mode at light load for high efficiency
  - Cycle-by-cycle current limit protection
  - Hic-cup mode output short circuit protection
  - Hic-cup mode output over voltage protection
- I²C compatible interface:
  - Supports 100kHz standard mode and 400kHz fast mode
  - 7-Bits VID programmable output voltage from 0.68V to 1.95V with 10mV/Step
  - VID voltage transition slew rate control
  - Power good status read back
  - Over temperature warning read back
  - On/Off control
- Thermal shutdown with auto recovery
- Input UVLO
- RoHS Compliant and Halogen Free
- Compact package: QFN3x3-20

Typical Applications

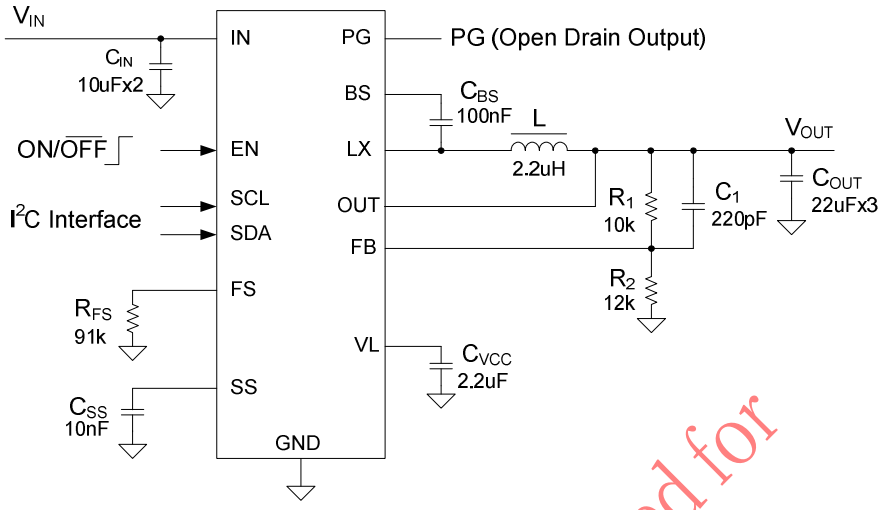
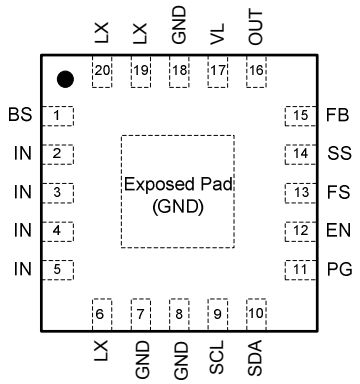


Figure 1. Schematic

Pinout (top view)



(QFN3x3-20)

Top Mark: AST*xyz*, (Device code: AST, ***x=year code, y=week code, z=lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Decouple this pin to LX with a 100nF capacitor
IN	2,3,4,5	Power supply input. Decouple this pin to GND with at least 10uF MLCC
LX	6,19,20	Inductor pin. Connect this pin to the switching node of inductor.
GND	7,8,18,EP	Ground pin.
SCL	9	Serial clock pin
SDA	10	Serial data pin.
PG	11	Open drain power good indicator. Externally pull high when the output is in regulation range. Otherwise pull low
EN	12	Enable control. Float to enable. This pin can also be used to adjust input UVLO with resistor divider
FS	13	Switching frequency setting pin. Connect a resistor from this pin to GND to adjust the switching frequency. F_{SW}(kHz)= 44350/R_{FS}, where R_{FS} is in kΩ.
SS	14	Soft-start input. Connect a capacitor from this pin to GND to program the soft-start time. A 5uA pull-up current source is connected to this pin. Tss(ms)=Css(nF)*0.6(V)/5(uA)
FB	15	Initial output voltage setting pin. Connect this pin to the resistor divider of the output
OUT	16	Output voltage sense pin
VL	17	Internal LDO output. Decouple this pin to GND with a 2.2uF ceramic capacitor

Absolute Maximum Ratings (Note 1)

IN, LX, EN, PG ---------- -0.3V to 20V
VL, BS-LX ---------- -0.3V to 4V
SDA, SCL ---------- -0.3V to 7V
OUT ---------- -0.3V to 7V
All other pins ---------- -0.3V to 4V
Power Dissipation,
P_D @ T_A = 25°C QFN3x3-20 ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA}, QFN3x3-20 ---------- 30°C/W
θ_{JC}, QFN3x3-20 ---------- 4.5°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 4.5V to 18V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN}=12V, V_{OUT} = 1.1V, L = 2.2uH, C_{OUT} = 3x22uF , T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		18	V
V_{UVLO_RISING}	$V_{UVLO,RISING}$	UVLO rising threshold voltage	4.00	4.25	4.50	V
$V_{UVLO\_FALLING}$	$V_{UVLO,FALLING}$	UVLO falling threshold voltage	3.50	3.75	3.95	V
Quiescent Current	I_Q	EN=High, FB=1V. Buck converters are not switching Mode='0'			500	μA
Shutdown Current	I_{SHUT}	EN =0			10	μA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
Buck Output Voltage Line Regulation	V_{LINE}	I_{OUT}=3A		0.5		%/V
Buck Output Voltage Load Regulation	V_{LOAD}	I_{OUT}=1~6A		0.5		%/A
Switching Frequency Program Range	$F_{OSC, RNG}$		200		1000	kHz
Switching Frequency Accuracy	F_{OSC}	R_{OSC}=88.7k	425	500	575	kHz
Soft-start Charging Current	I_{SS}			5		μA
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low		92.5		%V_{REF}
		V_{FB} rising, PG from low to high		95		%V_{REF}
		V_{FB} rising, PG from high to low		115		%V_{REF}
		V_{FB} falling, PG from high to low		110		%V_{REF}
Output OVP Threshold	V_{OVP}			120		%V_{REF}

Output OVP Response Time	t_{OVP}			20		µs
Output OVP Off Time	$t_{OFF, OVP}$			16		ms
Power Good Delay Time	T_{PG_F}	PG falling edge		250		µs
	T_{PG_R}	PG rising edge		2		ms
Power Good Low Voltage	V_{PG_LOW}	Sink 1mA to PG pin, FB=0.6V			0.4	V
Over Current Protection Wait Time	t_{WAIT}			500		µs
Over Current Protection Off Time	t_{OFF}			16		ms
Enable Logic High Threshold	V_{EN_HIGH}	Rising		1.2	1.26	V
Enable Logic Low Threshold	V_{EN_LOW}	Falling	1.1	1.15		V
Enable Pull-up Current	I_{EN}	V_{EN}=1V		2		µA
		V_{EN}=1.5V		6.55		µA
Minimum On Time	T_{ON_MIN}				100	ns
Maximum Duty Cycle	D_{MAX}			95		%
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown hysteresis	T_{HYS}			20		°C
Top FET R_{ON}	$R_{DS(ON),N11}$			50		mΩ
Bottom FET R_{ON}	$R_{DS(ON),N12}$			15		mΩ
Top FET Current Limit	$I_{LIM,TOP1}$			12		A
Bottom FET Current Limit	$I_{LIM,BOT1}$		6			
Bottom FET Reverse Current Limit	$I_{LIM,BOT2}$			-6		A
I^2C COMPATIBLE Interface						
Operating Frequemcy	f_{SCL}				400	kHz
SDA and SCL Input Logic Threshold	Logic low		0.9			V
	Logic high				2.5	V
SDA Output Low Voltage	$V_{OL,SDA}$				0.4	V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at TA = 25°C on a low effective 4-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of QFN3x3 packages is the case position for θJC measurement.

Note3: The following combination of inductor and output capacitor value is just used to improve start up.

Inductor	COUT
1.5uH	22uFx5ea
2.2uH	22uFx3ea

Note 4: The device is not guaranteed to function outside its operating conditions.

Block Diagram

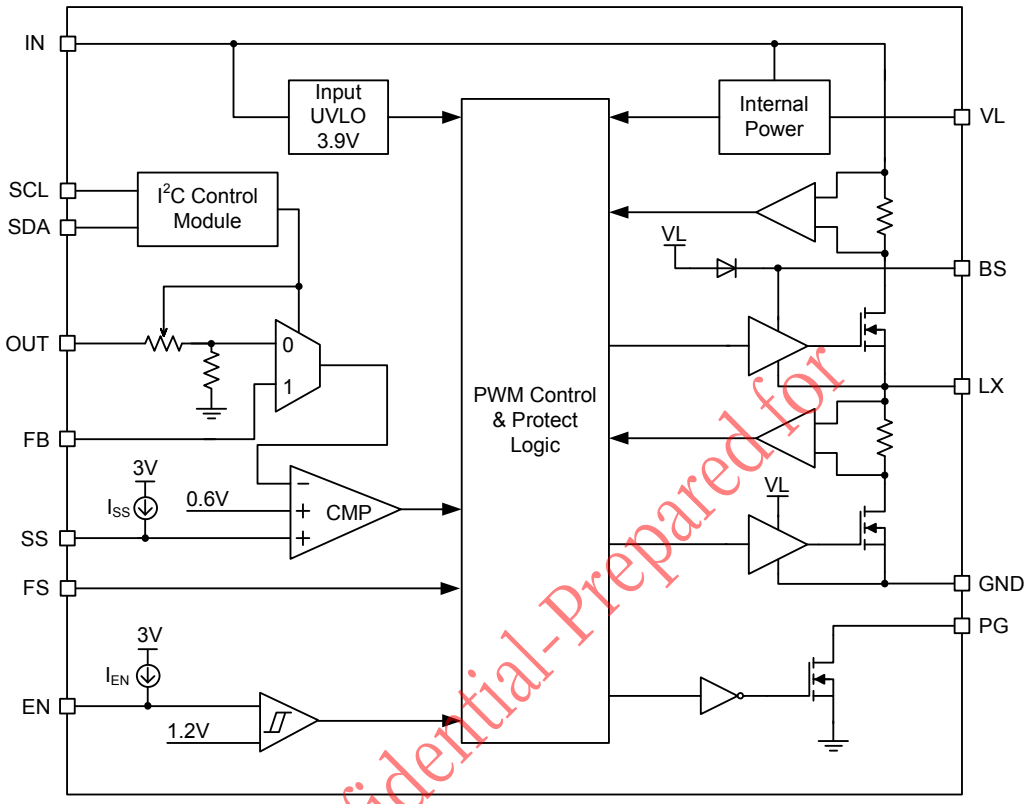


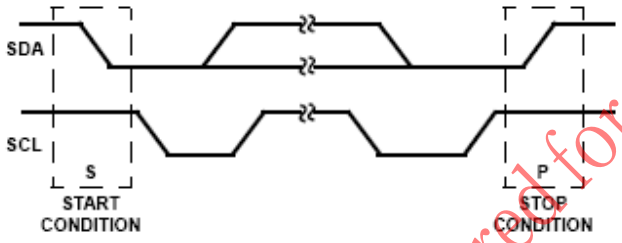
Figure 2. Block Diagram

I²C Compatible Interface

SY8106A integrates an I²C compatible interface works as a slave. The 7-bits device address is 0x65H
When SY8106A is in hardware shutdown (EN pin tied to ground), the device can't be updated via the I²C interface. And the registers are reset to default value. While in software shutdown (EN bit=0), the I²C interface is fully functional.

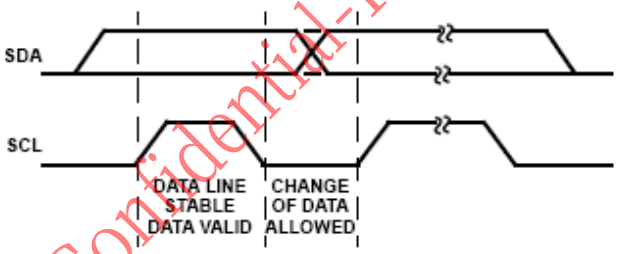
START and STOP Conditions:

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



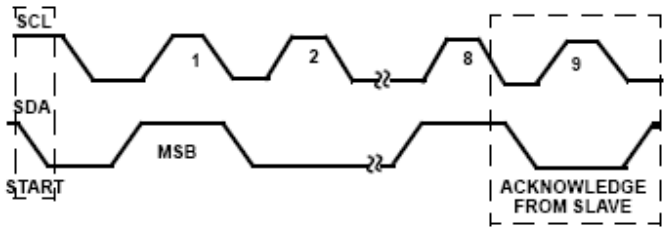
Data Validity:

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge:

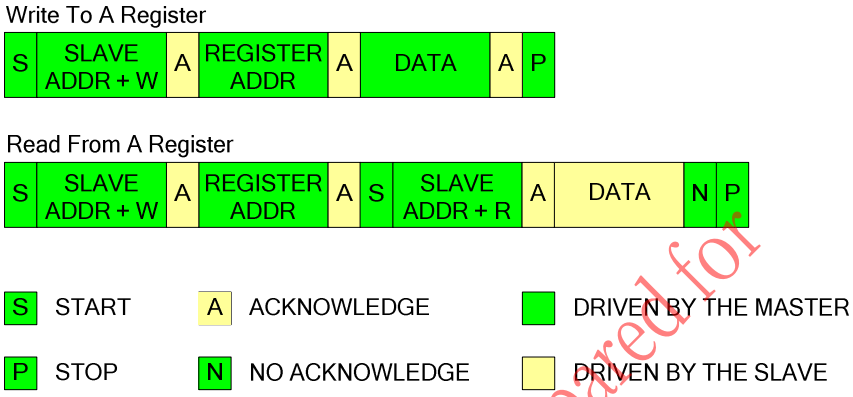
Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.



Data Transactions:

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START

condition, followed by 7-bits of slave address, followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the slave acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the slave which register the master will write or read. Once the slave receives a register address byte it responds with an acknowledge.



Register Settings:

1. VOUT1_SEL (0x01H)

Name	# of Bits	Access	Default	Description
VOUT_Bit7	7	R/W	0	Go bit, must set '1' to enable I²C voltage control
VOUT_Bit6	6	R/W	0	Channel 1 output voltage program, 10mV/Step 0x00H: 0.68V 0x7FH: 1.95V
VOUT_Bit5	5	R/W	0	
VOUT_Bit4	4	R/W	0	
VOUT_Bit3	3	R/W	0	
VOUT_Bit2	2	R/W	0	
VOUT_Bit1	1	R/W	0	
VOUT_Bit0	0	R/W	0	

2. VOUT_COM (0x02H)

Name	# of Bits	Access	Default	Description
	7	R/W	0	Reserved
Slew Rate 3	6	R/W	0	V_{OUT} slew rate control 000 : 10mV/cycle; 001: 10mV/2 cycles; 010: 10mV/4 cycles; 011 : 10mV/8 cycles; 100: 10mV/16 cycles; 101: 10mV/32 cycles;
Slew Rate 2	5	R/W	0	
Slew Rate 1	4	R/W	0	

				110 : 10mV/64cycles; 111: 10mV/128 cycles
	3	R/W	0	Reserved
	2	R/W	0	Reserved
Mode	1	R/W	0	0: Enable PSM operation at light load; 1: Force PWM operation
EN	0	R/W	0	0: Enable buck regulator; 1: Disabled buck regulator

3. SYS_STATUS (0x06H)

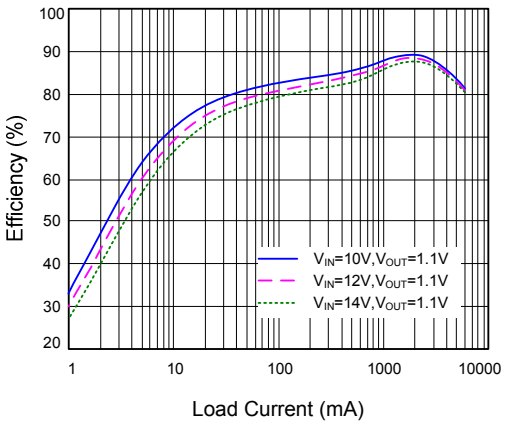
Name	# of Bits	Access	Default	Description
OTP	7	R	0	1: Die temperature over 160°C, OTP is triggered 0: OTP is not triggered
	6	R	0	Reserved
	5	R	0	Reserved
OC	4	R	0	1. OCP is triggered, and V_O drops below 1/3 of set point. 0. Current is below current limit
Temperature Warning (>125°C)	3	R	0	1: Die temperature over 125°C; 0: Die temperature below 125°C
	2	R	0	Reserved
	1	R	0	Reserved
PGOOD	0	R	0	1: V_{OUT} in power good regulation range 0: V_{OUT} not in power good regulation range

V_{OUT} Output Voltage Setting:

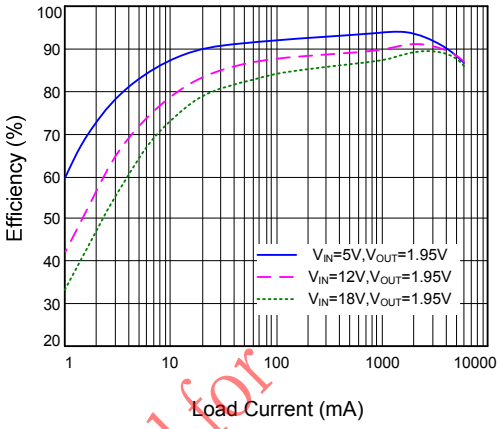
OUT_Bit [6:0]	VOUT (V)	OUT_Bit [6:0]	VOUT (V)	OUT_Bit [6:0]	VOUT (V)	OUT_Bit [6:0]	VOUT (V)
0x00	0.68	0x20	1.00	0x40	1.32	0x60	1.64
0x01	0.69	0x21	1.01	0x41	1.33	0x61	1.65
0x02	0.70	0x22	1.02	0x42	1.34	0x62	1.66
0x03	0.71	0x23	1.03	0x43	1.35	0x63	1.67
0x04	0.72	0x24	1.04	0x44	1.36	0x64	1.68
0x05	0.73	0x25	1.05	0x45	1.37	0x65	1.69
0x06	0.74	0x26	1.06	0x46	1.38	0x66	1.70
0x07	0.75	0x27	1.07	0x47	1.39	0x67	1.71
0x08	0.76	0x28	1.08	0x48	1.40	0x68	1.72
0x09	0.77	0x29	1.09	0x49	1.41	0x69	1.73
0x0A	0.78	0x2A	1.10	0x4A	1.42	0x6A	1.74
0x0B	0.79	0x2B	1.11	0x4B	1.43	0x6B	1.75
0x0C	0.80	0x2C	1.12	0x4C	1.44	0x6C	1.76
0x0D	0.81	0x2D	1.13	0x4D	1.45	0x6D	1.77
0x0E	0.82	0x2E	1.14	0x4E	1.46	0x6E	1.78
0x0F	0.83	0x2F	1.15	0x4F	1.47	0x6F	1.79
0x10	0.84	0x30	1.16	0x50	1.48	0x70	1.80
0x11	0.85	0x31	1.17	0x51	1.49	0x71	1.81
0x12	0.86	0x32	1.18	0x52	1.50	0x72	1.82
0x13	0.87	0x33	1.19	0x53	1.51	0x73	1.83
0x14	0.88	0x34	1.20	0x54	1.52	0x74	1.84
0x15	0.89	0x35	1.21	0x55	1.53	0x75	1.85
0x16	0.90	0x36	1.22	0x56	1.54	0x76	1.86
0x17	0.91	0x37	1.23	0x57	1.55	0x77	1.87
0x18	0.92	0x38	1.24	0x58	1.56	0x78	1.88
0x19	0.93	0x39	1.25	0x59	1.57	0x79	1.89
0x1A	0.94	0x3A	1.26	0x5A	1.58	0x7A	1.90
0x1B	0.95	0x3B	1.27	0x5B	1.59	0x7B	1.91
0x1C	0.96	0x3C	1.28	0x5C	1.60	0x7C	1.92
0x1D	0.97	0x3D	1.29	0x5D	1.61	0x7D	1.93
0x1E	0.98	0x3E	1.30	0x5E	1.62	0x7E	1.94
0x1F	0.99	0x3F	1.31	0x5F	1.63	0x7F	1.95

Typical Performance Characteristics

Efficiency vs. Load Current

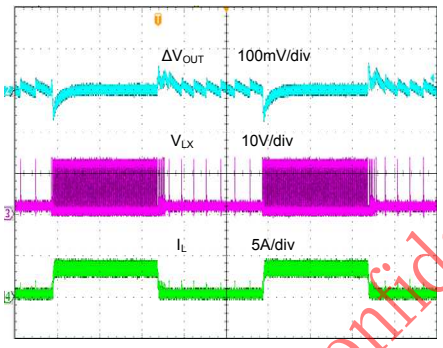


Efficiency vs. Load Current



Load Transient

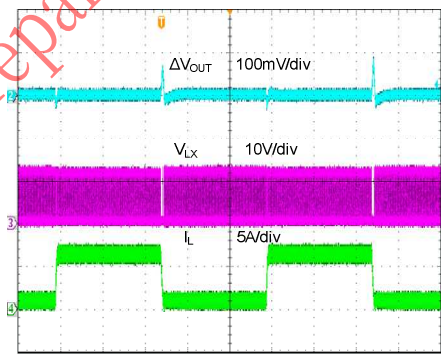
(V_{IN}=12V, V_{OUT}=1.1V, I_O=0 ~ 3A)



Time (200μs/div)

Load Transient

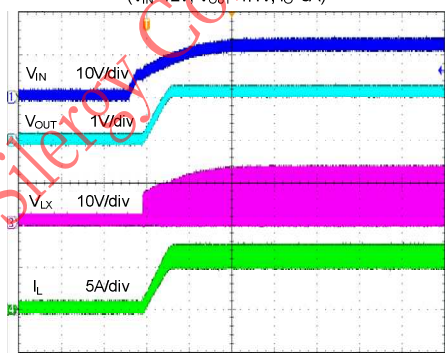
(V_{IN}=12V, V_{OUT}=1.1V, I_O=0.6 ~ 6A)



Time (200μs/div)

Startup from V_{IN}

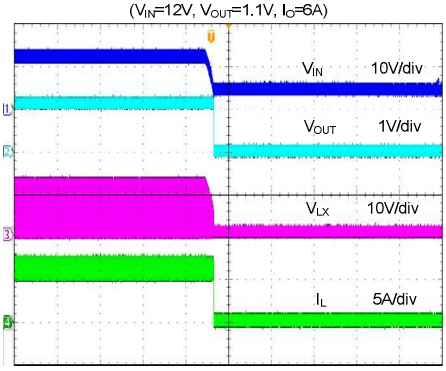
(V_{IN}=12V, V_{OUT}=1.1V, I_O=6A)



Time (2ms/div)

Shutdown from V_{IN}

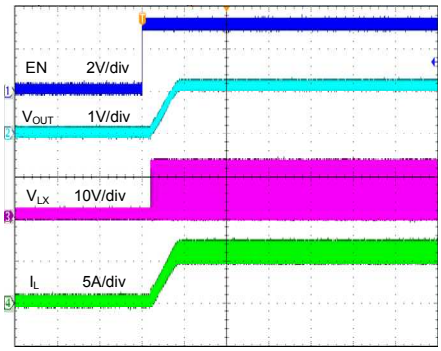
(V_{IN}=12V, V_{OUT}=1.1V, I_O=6A)



Time (10ms/div)

Startup from Enable

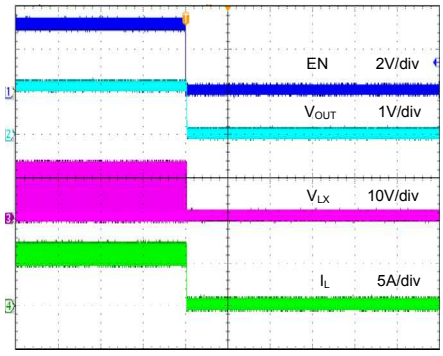
(V_{IN}=12V, V_{OUT}=1.1V, I_O=6A)



Time (2ms/div)

Shutdown from Enable

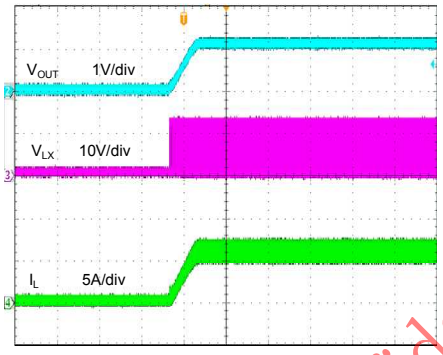
(V_{IN}=12V, V_{OUT}=1.1V, I_O=6A)



Time (2ms/div)

Startup from I²C

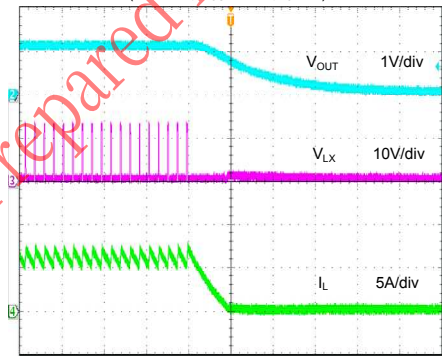
(V_{IN}=12V, V_{OUT}=1.1V, I_O=6A)



Time (2ms/div)

Shutdown from I²C

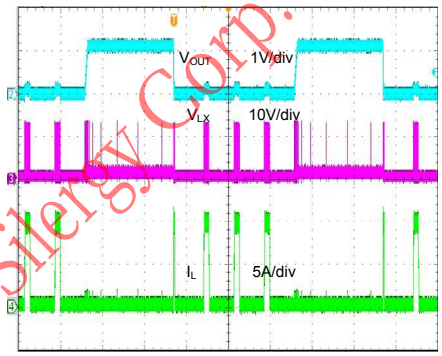
(V_{IN}=12V, V_{OUT}=1.1V, I_O=6A)



Time (10μs/div)

Short Circuit Protection

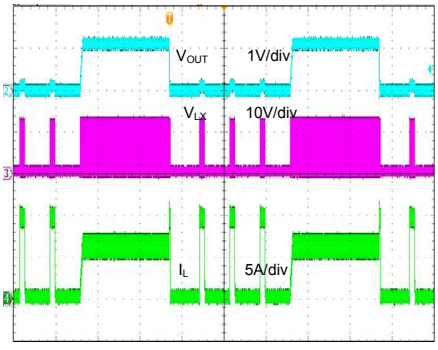
(V_{IN}=12V, V_{OUT}=1.1V, Null Load to short)



Time (20ms/div)

Short Circuit Protection

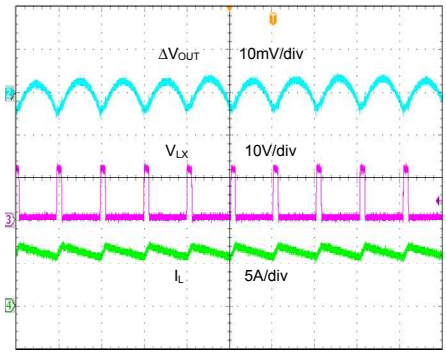
(V_{IN}=12V, V_{OUT}=1.1V, 6A to short)



Time (20ms/div)

Output Ripple

(V_{IN}=12V, V_{OUT}=1.1V, I_O=6A)



Time (2μs/div)

Operation

SY8106A develops a high efficiency synchronous buck regulator capable of delivering 6A output current. The device operates over a wide input voltage range from 4.5V to 18V. SY8106A adopts instant PWM architecture to achieve fast transient response. The switching frequency is adjustable from 200kHz to 1MHz.

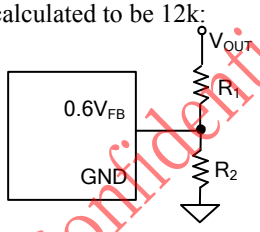
SY8106A integrates an I^2C compatible interface for output voltage setting, status read back, etc. The device also features enable control, open drain power good indicator, cycle-by-cycle current limit, short circuit protection and thermal shutdown.

Applications Information

Feedback resistor dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 1.1V, R_1=10k is chosen, then using following equation, R_2 can be calculated to be 12k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT\_MAX} \cdot \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10uF low ESR ceramic capacitor is recommended.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, an X5R or better grade ceramic capacitor greater than 44uF capacitance can work well. The capacitance derating with DC voltage must be considered.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8106A regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected greater than the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN\_MAX})}{F_{SW} \times L \times 2}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with smaller DCR to achieve a good overall efficiency.

Soft start time programming and output voltage tracking:

Connect a capacitor from SS pin to GND to program the soft-start time. A 5uA pull-up current source is connected to SS pin. The soft start time can be calculated by below equation:

$$T_{SS}(ms) = C_{SS}(nF) \times \frac{0.6(V)}{5(uA)}$$

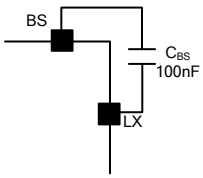
When external voltage on SS pin is less than the internal 0.6V reference voltage, the buck output voltage will track this external voltage during soft start.

Power Good Indication

PG is an open drain output. This pin is externally pulled high when the FB voltage is within 95% to 115% of the internal reference voltage. Otherwise is pulled low.

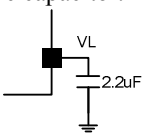
External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



VL LDO

The 3.3V VL LDO provides the power supply for internal control circuit. Bypass this pin to ground with a 2.2uf ceramic capacitor.



Switching Frequency Setting:

Connect a resistor from FS pin to GND to adjust the switching frequency. The switching frequency is adjustable from 200kHz to 1MHz. The switching frequency can be calculated by below equation:

$$F_{SW}(kHz) = \frac{44350}{R_{FS}}$$

Where R_{FS} is in kΩ.

Layout Design:

The layout design of SY8106A regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, C_{VL} L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) C_{VL} should be placed close to VL pin and GND pin

5) The components R_1 and R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

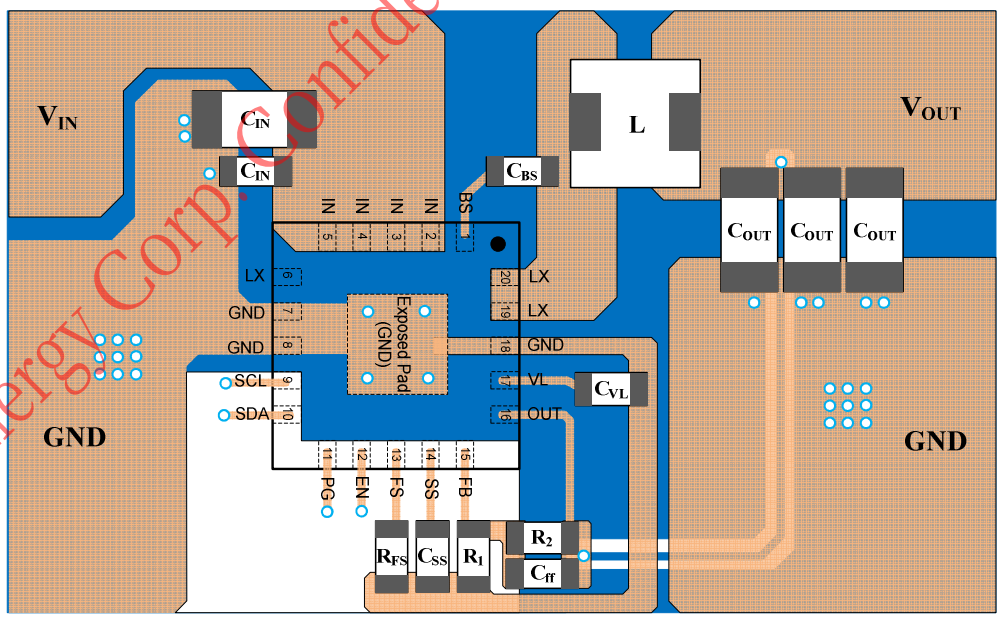
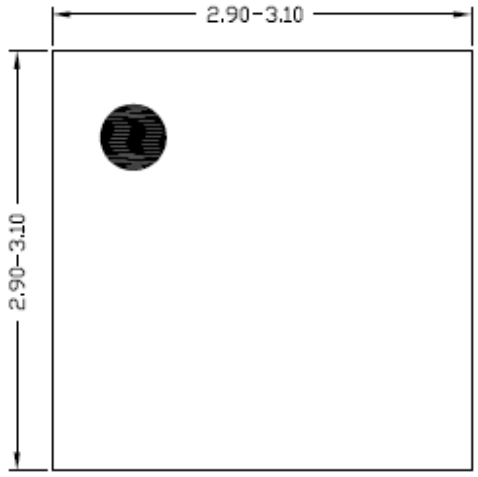


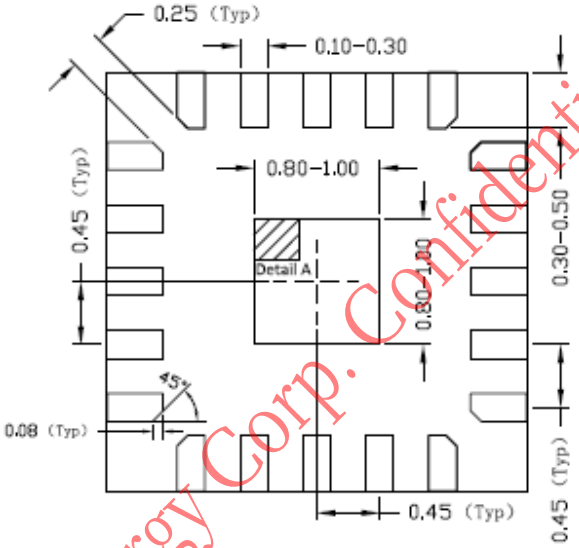
Figure 3. PCB Layout Suggestion

QFN3x3-20 Outline Drawing

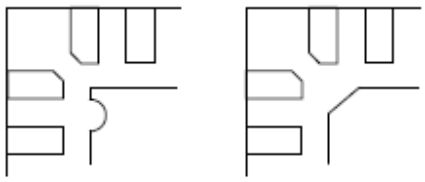


Top View

Side View



Bottom View

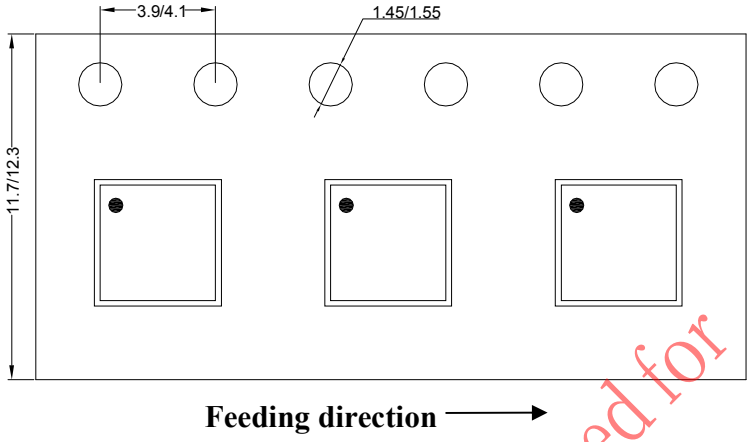


Detail A
Pin1 Identifier: two options

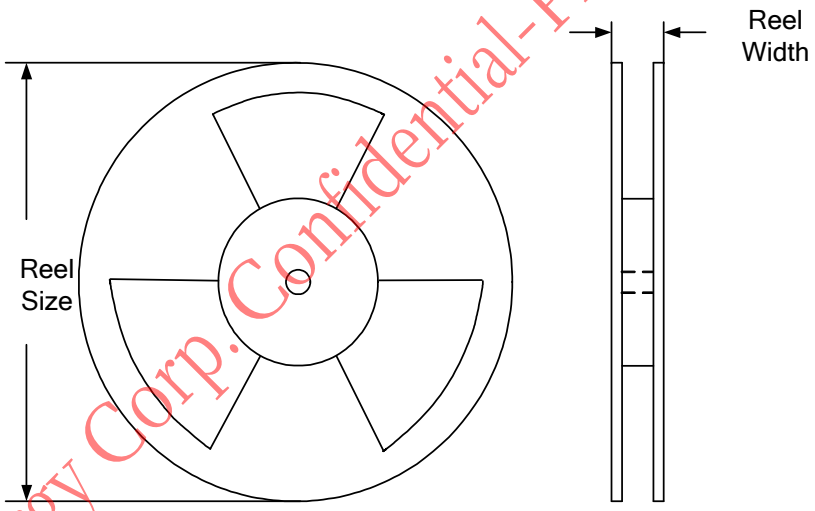
Notes: **All dimension in MM and exclude mold flash & metal burr**

Taping & Reel Specification

1. QFN3x3-20 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	12.4	400	400	5000

3. Others: NA