RTL8187SE-GR

SINGLE-CHIP IEEE 802.11b/g WLAN CONTROLLER w/PCI EXPRESS INTERFACE

DATASHEET

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This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/01/31	First release.

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek RTL8187SE is a low-profile highly integrated cost-effective Single-Chip Wireless LAN network interface controller that integrates a Wireless LAN MAC, a baseband processor, and 2.4GHz RF onto one chip. It provides a PCI Express bus controller, and full compliance with IEEE 802.11 and IEEE 802.11b/g specifications. It also complies with WMM, 802.11e, and CCX specifications.

To reduce protocol overhead, the RTL8187SE supports Short InterFrame Space (SIFS) burst mode to send packets back-to-back. A protection mechanism prevents collisions among 802.11b nodes.

Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK), and Orthogonal Frequency Division Multiplexing (OFDM) baseband processing are implemented to support all IEEE 802.11b, and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, along with complementary code keying to provide data rates of 1, 2, 5.5, and 11Mbps, with long or short preamble. A high-speed Fast Fourier Transform (FFT)/Inverse Fast Fourier Transform (IFFT), combined with BPSK, QPSK, 16QAM and 64QAM modulation of the individual sub-carriers, provides data rates of 6, 9, 12, 18, 24, 36, 48 and 54Mbps, with rate-compatible punctured convolutional coding with a coding rate of 1/2, 2/3, and 3/4.

An enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder are built-in to alleviate severe multipath effects. Efficient IQ-imbalance calibration, DC offset, phase noise, frequency offset, and timing offset compensation reduce radio frequency front-end impairments. Selectable digital transmit and receive FIR filters are provided to meet the requirements of transmit spectrum masks, and to reject adjacent channel interference, respectively. Both in the transmitter and receiver, programmable scaling in the digital domain trades the qµAntization noise against the increased probability of clipping. Robust signal detection, symbol boundary detection, and channel estimation perform well at the minimum sensitivity.

The RTL8187SE supports fast receiver Automatic Gain Control (AGC) and antenna diversity functions, and an adaptive transmit power control function to obtain better performance in the analog portions of the transceiver. It also has on-chip digital-to-analog converters and analog-to-digital converters for analog I and Q inputs and outputs, transmit TSSI and receiver RSSI inputs, and transmit and receiver AGC outputs.

It supports Advanced Configuration Power management Interface (ACPI), Legacy PCI power management, and PCI Express power management for modern operating systems that are capable of Operating System directed Power Management (OSPM). PCI MSI (Message Signaled Interrupt) function and PCI Express Device Serial Number Capability are also supported.

In addition to the ACPI feature, the RTL8187SE also supports remote wake-up (including AMD Magic Packet and Microsoft® wake-up frame) in both ACPI and APM environments. To support Wake on Wireless LAN from a deep power down state (e.g., D3cold, i.e. main power is off and only auxiliary power exists), the auxiliary power source must be able to provide the needed power. When auxiliary power is applied and the main power remains off, the RTL8187SE is ready and waiting for a Magic Packet or wake-up frame to wake the system up.

The RTL8187SE supports an enhanced link list descriptor-based buffer management architecture, which is an essential part of a design for a modern network interface card. It contributes to lowering CPU utilization. Also, the RTL8187SE features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low pin count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure. Support is also provided for Multiple BSSID, Adjustable fallback steps and fallback rates during auto rate fallback, TX Power Tracking, Enhanced three-wire mechanism, Parallel Control Interface between Baseband and RF, and Bluetooth coexistence.

The RTL8187SE keeps network maintenance costs low and eliminates usage barriers. The RTL8187SE is highly integrated and requires no ‘glue’ logic or external memory.

2. Features

- 64-Pin QFN with ‘Green’ package
- State machine implementation without external memory (RAM, flash) requirement
- Complies with IEEE 802.11b/g standards
- Supports descriptor-based buffer management
- Integrated Wireless LAN MAC and Direct Sequence Spread Spectrum/OFDM Baseband Processor in one chip
- Enhanced signal detector, adaptive frequency domain equalizer, and soft-decision Viterbi decoder to alleviate severe multipath effects
- Processing Gain compliant with FCC
- On-Chip A/D and D/A converters for I/Q Data, AGC, and Adaptive Power Control
- Supports both transmit and receive Antenna Diversity
- Data rates of 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54Mbps
- Supports 40MHz OSC as the internal clock source. The frequency deviation of the OSC must be within 25ppm on IEEE 802.11g
- PCI Express bus controller
  - Complies with PCI Express 1.1 and PCI Express Mini Card Electromechanical Specification Revision 1.1
  - PCI power management Revision 1.2
  - Supports PCI Express Active State Power Management (ASPM)
  - Provides PCI Express bus data transfers and PCI Express memory space or IO space mapped data transfers of the RTL8187SE’s operational registers
  - Supports ACPI (Rev 1.0, 1.0b, 2.0)
- Supports Wake-On-WLAN (WoWLAN) function and remote wake-up (Magic Packet and Microsoft® wake-up frame)
- Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI Express configuration space
- IEEE 802.11g protection mechanisms for both RTS/CTS and CTS-to-self
- Burst-mode support for dramatically enhanced throughput
- DSSS with DBPSK and DQPSK, CCK modulations and demodulations supported with long and short preamble
- OFDM with BPSK, QPSK, 16QAM and 64QAM modulations and demodulations supported with rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, and 3/4
- Efficient IQ-imbalance calibration, DC offset, phase noise, frequency offset and timing offset compensation reduce analog front-end impairments
- Selectable digital transmit and receiver FIR filters provided to meet transmit spectrum mask requirements and to reject adjacent channel interference

- Programmable scaling both in transmitter and receiver to trade qμAntization noise against the increased probability of clipping
- Fast receiver Automatic Gain Control (AGC) & antenna diversity functions
- Adaptive transmit power control function
- Complies with WMM, 802.11e, and CCX specifications
- Complies with 802.11i and 802.11j specifications
- Hardware-based IEEE 802.11i encryption/decryption engine, including 64-bit/128-bit WEP, TKIP, and AES
- Supports Wi-Fi alliance WPA and WPA2 security
- Supports a 32-bit general-purpose timer
- Contains two large independent transmit and receive FIFO buffers
- Advanced power saving mode when the LAN and wakeup function are not used
- Uses 93C46 (64*16-bit EEPROM) or 93C56 (128*16-bit EEPROM) to store resource configuration and ID parameter data
- LED pins for various network activity indications
- Nine GPIO pins supported
- Supports digital loopback capability on both ports
- Flexible RF transceiver interface for different RF transceiver applications
- Built-in 3.3V to 1.8V regulator
- 3.3V power supply required
- 0.18μm CMOS process

3. System Applications

- Wireless PCI Express adapter
- Wireless notebook Mini Card adapter
- Wireless system (wireless gateway router, wireless ADSL router, wireless set-top box etc.) with PCI Express or Mini Card slot

4. Block Diagrams

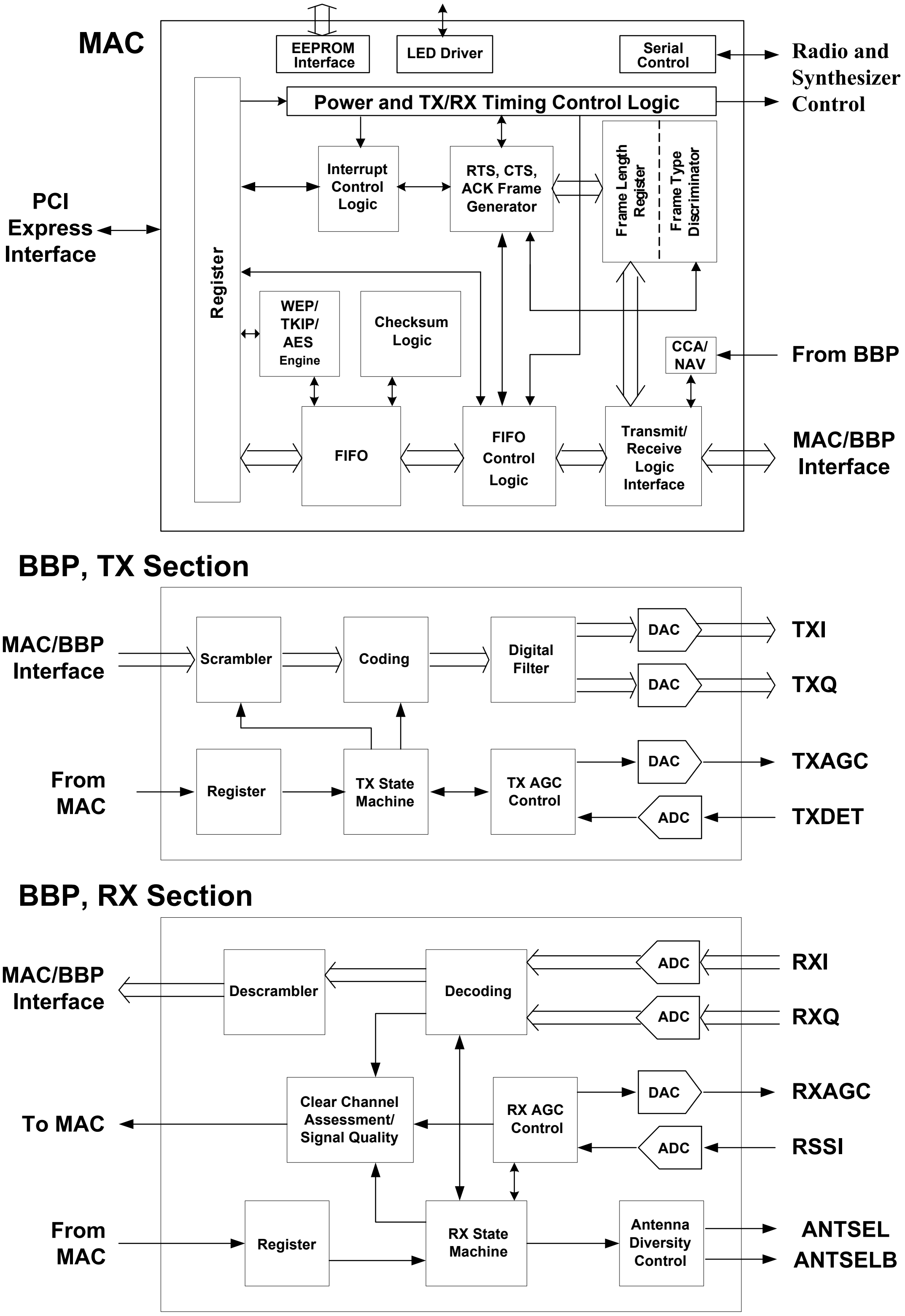


Figure 1. Block Diagram

RF Diagram

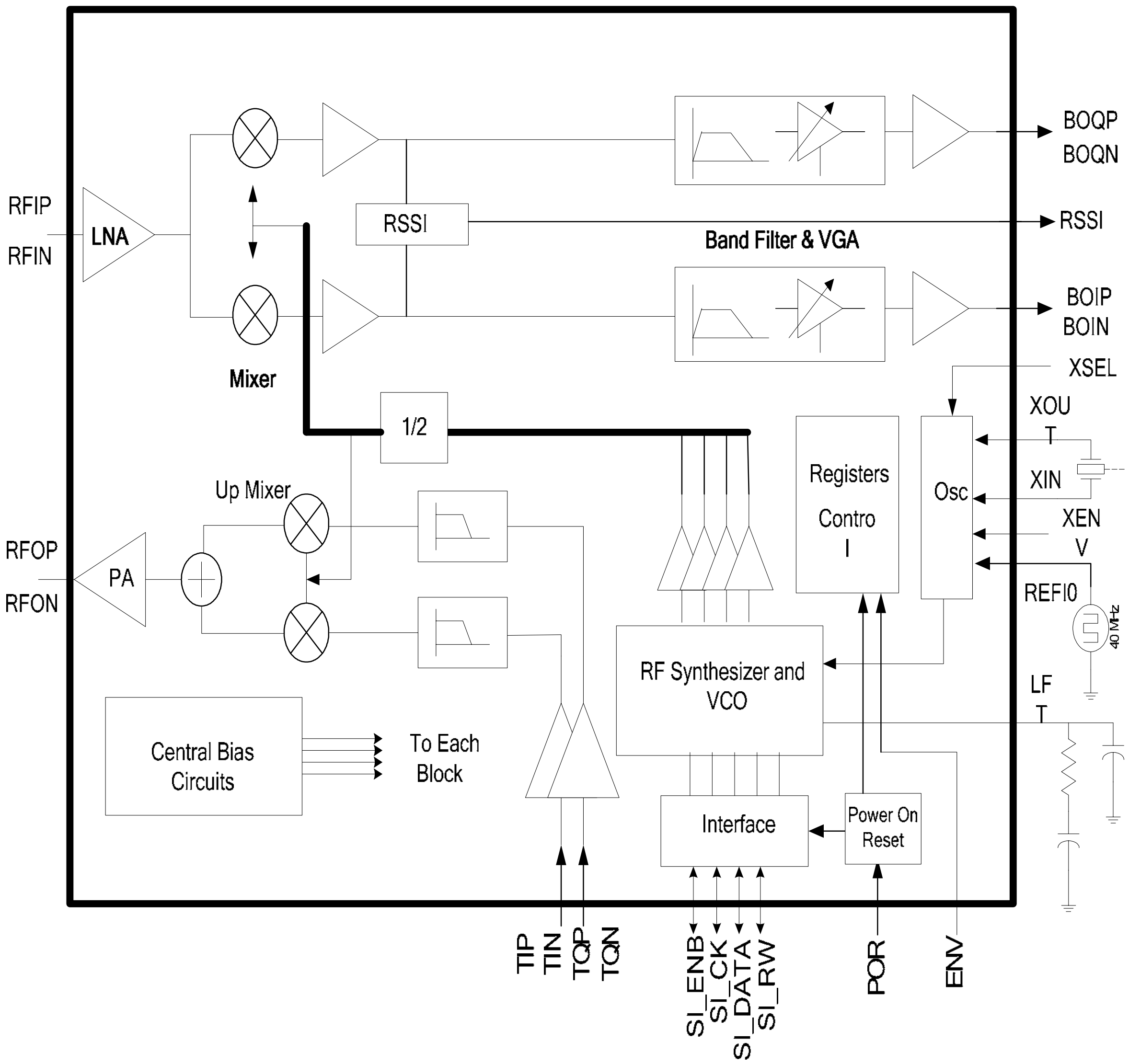


Figure 2. RF Block Diagram

5. Pin Assignments

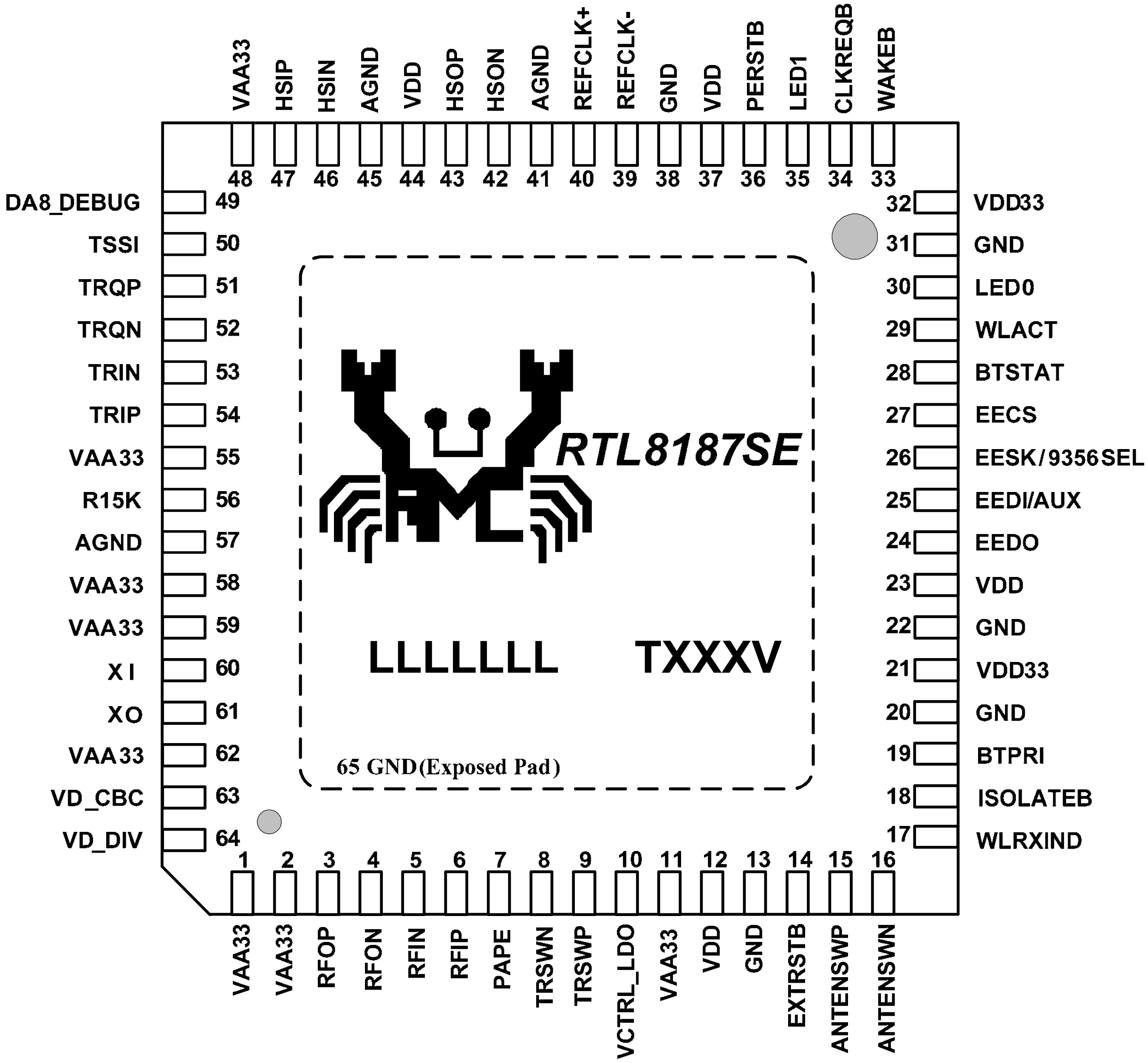


Figure 3. Pin Assignments

5.1. Package Identification

Green package is indicated by a ‘G’ in the location marked ‘T’ in Figure 3.

6. Pin Descriptions

The following signal type codes are used in the tables:

I:	Input	AO:	Analog Output
DI:	Digital Input	AIO:	Analog Input/Output
AI:	Analog Input	T/S:	Tri-State Bi-Directional Input/Output
O:	Output	S/T/S:	Sustained Tri-State
DO:	Digital Output	O/D:	Open Drain

6.1. Power Management/Isolation Interface

Table 1. Power Management/Isolation Interface

Symbol	Type	Pin No	Description
WAKEB	O/D	33	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	DI	18	Isolate Pin: Active low. Used to isolate the RTL8187SE-GR from the PCI Express bus. The RTL8187SE-GR will not drive its PCI Express outputs (excluding WAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

6.2. PCI Express Interface

Table 2. PCI Express Interface

Symbol	Type	Pin No	Description
REFCLK+	I	40	PCI Express Differential Reference Clock Source: 100MHz ±300ppm.
REFCLK-	I	39	
HSOP	O	43	PCI Express Transmit Differential Pair.
HSON	O	42	
HSIP	I	47	PCI Express Receive Differential Pair.
HSIN	I	46	
PERSTB	I	36	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8187SE-GR returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	O/D	34	Reference Clock Request Signal. This signal is used by the RTL8187SE-GR to request starting of the PCI Express reference clock.

6.3. EEPROM Interface

Table 3. EEPROM Interface

Symbol	Type	Pin No	Description
EESK/9356SEL	DO/DI	26	EESK in 93C46 (93C56) programming or auto-load mode. Input Pin as 9356 Select Pin at Initial Power-up. When this pin is pulled high with a 10K resistor, the 93C56 EEPROM is used to store the resource data for the RTL8187SE. The RTL8187SE latches the status of this pin at power-up to determine which EEPROM (93C46 or 93C56) is used. After power on and GPIO_EN[5]=1, this pin is GPIO[5].
EEDI/AUX	DO/DI	25	EEDI: Output to serial data input pin of EEPROM. AUX: Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8187SE assumes that no Aux. Power exists. After power on and GPIO_EN[4]=1, this pin is GPIO[4].
EEDO	DI	24	This pin is GPIO[3] after power on and GPIO_EN[3]=1, otherwise, it is EEDO in 93C46 (93C56) programming or auto-load mode.
EECS	DO	27	EEPROM Chip Select. 93C46 (93C56) chip select.

6.4. Power Pins

Table 4. Power Pins

Symbol	Type	Pin No	Description
VDD33	P	21, 32	+3.3V (Digital).
VAA33	P	1, 2, 11, 48, 55, 58, 59, 62	+3.3V (Analog).
VDD	P	12, 23, 37, 44	+1.8V.
GND	P	13, 20, 22, 31, 38, 65	Ground (Digital).
AGND	P	41, 45, 57	Ground (Analog).
VCTRL_LDO	AO	10	Reserve this pin for external BJT option to generate 1.8V for digital core circuit.
VD_CBC	P	63	Reserved for external power transistor.
VD_DIV	P	64	Reserved for external power transistor.

6.5. LED Interface

Table 5. LED Interface

Symbol	Type	Pin No	Description
LED0	O	30	LED Pin. a. PWRON: I2C_CK b. After PWRON & LED_CONTROL=3'h7: GPIO[0] c. Other: LED0
LED1	O	35	LED Pin. a. PWRON: I2C_IO b. After PWRON & LED_CONTROL=3'h7: GPIO[1] c. Other: LED1

6.6. Baseband and RF Pins

Table 6. Baseband and RF Pins

Symbol	Type	Pin No	Description
RFOP	AO	3	2.4GHz Differential RF Power Amplifier Output.
RFON	AO	4	
RFIN	AI	5	2.4GHz Differential RF Input.
RFIP	AI	6	
PAPE	DO	7	Enable Control for Optional External Power Amplifier
TRSWN	DO	8	Control Signals for Optional External RF T/R Switch
TRSWP	DO	9	
ANTENSWP	DO	15	Control Signals for Antenna Switch
ANTENSWN	DO	16	
TSSI	AI	50	Transmit Signal Strength Indication From External Power Amplifier
TRQP	AIO	51	Via register setting, can be programmed to one of the following four types of pins: RF TXQP: Input pin for RF TX test RF RXQP: Output pin for RF RX test AFE TXQP: Output pin for DAC test AFE RXQP: Input pin for ADC test
TRQN	AIO	52	Via register setting, can be programmed to one of the following four types of pins: RF TXQN: Input pin for RF TX test RF RXQN: Output pin for RF RX test AFE TXQN: Output pin for DAC test AFE RXQN: Input pin for ADC test
TRIN	AIO	53	Via register setting, can be programmed to one of the following four types of pins: RF TXIN: Input pin for RF TX test RF RXIN: Output pin for RF RX test AFE TXIN: Output pin for DAC test AFE RXIN: Input pin for ADC test
TRIP	AIO	54	Via register setting, can be programmed to one of the following four types of pins: RF TXIP: Input pin for RF TX test RF RXIP: Output pin for RF RX test AFE TXIP: Output pin for DAC test AFE RXIP: Input pin for ADC test

6.7. Bluetooth Co-Existence Pins

Table 7. Bluetooth Co-Existence Pins

Symbol	Type	Pin No	Description
WLRXIND	O	17	Wireless LAN RX Activity Indicator
BTPRI	IO	19	Bluetooth Priority Pin This pin is GPIO[2] after power on and GPIO_EN[2]=1, otherwise, this pin is BTPRI. The BTPRI signal indicates when an important Bluetooth packet is being transmitted or received.
BTSTAT	IO	28	Bluetooth Status This pin is GPIO[6] after power on and GPIO_EN[6]=1, otherwise, this pin is BTSTAT. The BTSTAT signal indicates when normal Bluetooth packets are being transmitted or received.
WLACT	O	29	WLAN Activity The WLAN_Active signal indicates when WLAN is either transmitting or receiving in the 2.4GHz ISM band.

6.8. Clock and Other Pins

Table 8. Clock and Other Pins

Symbol	Type	Pin No	Description
R15K	IO	56	This pin must be pulled low by a 15K Ω resistor.
XI	I	60	Input of 40MHz Clock Reference.
XO	O	61	Output of 40MHz Clock Reference.
EXTRSTB	I	14	External Reset Pin: Active Low.
DA8_DEBUG	O	49	Debug Pin.

7. EEPROM (93C46 or 93C56) Contents

The RTL8187SE supports the attachment of an external EEPROM. The 93C46 is a 1Kbit EEPROM (the 93C56 is a 2Kbit EEPROM). The EEPROM interface provides the ability for the RTL8187SE to read from, and write data to, an external serial EEPROM device. Values in the external EEPROM allow default fields in PCI configuration space and IO space to be overridden following an internal power on reset, or software EEPROM auto-load command. The RTL8187SE will auto-load values from the EEPROM to these fields in configuration space and IO space. If the EEPROM is not present, the RTL8187SE initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using ‘bit-bang’ accesses via the 9346CR Register.

Note: It is suggested to obtain Realtek approval before changing the default settings of the EEPROM.

8. PCI EXPRESS

8.1. PCI EXPRESS Bus Interface

The RTL8187SE is compliant with PCI Express™ Base Specification Revision 1.1, and runs at 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pairs. The RTL8187SE supports 4 types of PCI Express messages; interrupt messages, error messages, power management messages, and hot-plug messages. PCI Express lane polarity reversal and link reversal are also supported to ease PCB layout constraints.

8.1.1. PCI Express Transmitter

The RTL8187SE's PCI Express block receives digital data recovered from the WLAN MAC interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by sacrificing the 25 percent overhead to the system through the addition of 2 extra bits. Then, the data code groups are passed through its serializer for packet framing to generate 2.5 Gbps serial data and transmitted onto PCB trace to its upstream device via differential driver.

8.1.2. PCI Express Receiver

The RTL8187SE's PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are resynchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data descrambling, the original digital data is able to be recovered and then the data is passed to the RTL8187SE's internal WLAN MAC to be transmitted on the air.

8.2. PCI Configuration Space Table

Note: The following table assumes Power Management is enabled.

Table 9. PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	0	0	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	IntDisable	0	SERREN
		W	-	-	-	-	-	IntDisable	-	SERREN
06h	Status	R	0	0	0	1	IntSt	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	0	0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	1	0	0	0	1	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	1	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	RW	CLS7	CLS6	CLS5	CLS4	CLS3	CLS2	CLS1	CLS0
0Dh	LTR	R	0	0	0	0	0	0	0	0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		RW	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		RW	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		RW	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h-17h	Reserved									
18h-1Fh	Reserved									
20h-27h	Reserved									
28h-2Bh	Reserved									
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		RW	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		RW	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	0	1	0	0	0	0	0	0
35h-3Bh	Reserved									
3Ch	ILR	RW	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	0	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Fh	MXLAT	R	0	0	0	0	0	0	0	0
40h	PMID	R	0	0	0	0	0	0	0	1
41h	NextPtr	R	0	1	0	1	0	0	0	0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
43h		R	PME_D3$_{cold}$	PME_D3$_{hot}$	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
44h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
45h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
46-4Fh	Reserved									
50h	MSIID	R	0	0	0	0	0	1	0	1
51h	NextPtr	R	0	1	1	1	0	0	0	0
52h	Message Control	R	64-bit Address Capable	Multiple Message Enable			0	0	0	MSI Enable
		W	-	Multiple Message Enable			-	-	0	MSI Enable
53h		Reserved. Always return 0								
54h-57h	Message Address Low	RW	64-bit Interrupt Message Address Low							
58h-5Bh	Message Address High	RW	64-bit Interrupt Message Address High							
5Ch-5Dh	Message Data	RW	16-bit Message Data							
5E-6Fh	RESERVED									
70h	PCIEID	R	0	0	0	1	0	0	0	0
71h	NextPtr	R	0	0	0	0	0	0	0	0
72h-73h	PCIE Cap.	R	0	0	0	Legacy	0	0	0	1
		R	0	0	0	0	0	0	0	0
74h-77h	Device Capability Register	R	L0s_acpt_latency[1]	L0s_acpt_latency[0]	Entend_tag_support	0	0	Max_payload_size_support		
		R	Role Base Error rpt	0	0	0	L1_acpt_latency[2]	L1_acpt_latency[1]	L1_acpt_latency[0]	L0s_acpt_latency[2]
		R	0	0	0	0	0	0	0	0
		R	0	0	0	0	0	0	0	0
78h-79h	Device Control Register	RW	Max_payload_size			Relaxed_ordering_en	Unsupport_rqst_rpt_en	Fatal_err_rpt_en	Non_fatal_err_rpt_en	Correctable_err_rpt_en
		RW	0	Max_read_request_size			No_snoop_en	Auxpwr_PM_en	0	Entend_tag_en
7Ah	Device Status Register	R	0	0	Transact_ion_pending	AuxPwr_det	Upsupport_rqst_det	Fatal_err_det	Non_fatal_err_det	Correctable_err_det
		W	0	0	-	-	Upsupport_rqst_det	Fatal_err_det	Non_fatal_err_det	Correctable_err_det
7Bh		R	0	0	0	0	0	0	0	0
7Ch	Link Capability Register	R	0	0	0	1	0	0	0	1
7Dh		R	L1_exit_lat[0]	L0s_exit_lat[2]	L0s_exit_lat[1]	L0s_exit_lat[0]	ASPM_support		0	0
7Eh		R	0	0	0	0	0	Clock_PM	L1_exit_lat[2]	L1_exit_lat[1]0
7Fh		R	0	0	0	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
80h	Link Control Register	R	Extended_ sync	Common_ clock	0	0	RCB	0	ASPM_control	
		W	Extended_ sync	Common_ clock	0	0	RCB	0	ASPM_control	
81h		R	0	0	0	0	0	0	0	Enable clock_PM
		W	0	0	0	0	0	0	0	Enable clock_PM
82h	Link Status Register	R	0	0	0	1	0	0	0	1
83h		R	0	0	0	Slot_clock_ cfg	0	0	0	0
84h	Slot Capability Register	R	Slot power Limit[0]	Hot-Plug Capable	Hot-Plug Surprise	Power indicator present	Attn indicator present	MRL sensor present	Power control present	Attn button present
85h		R	Slot power Limit scale[0]	Slot power Limit[7]	Slot power Limit[6]	Slot power Limit[5]	Slot power Limit[4]	Slot power Limit[3]	Slot power Limit[2]	Slot power Limit[1]
86h		R	Physical slot Number[4]	Physical slot Number[3]	Physical slot Number[2]	Physical slot Number[1]	Physical slot Number[0]	No common Complete support	Electromechanical interlock present	Slot power Limit scale[1]
87h		R	Physical slot Number[12]	Physical slot Number[11]	Physical slot Number[1]	Physical slot Number[9]	Physical slot Number[8]	Physical slot Number[7]	Physical slot Number[6]	Physical slot Number[5]
88h	Slot Control Register	RW	Attn Indicator Control[1]	Attn Indicator Control[0]	Hot-Plug Interrupt Enable	Command Completed interrupt Enable	Presence Detect Changed Enable	MRL Sensor Changed Enable	Power Fault Detected Enable	Attn Bottom Pressed Enable
89h		RW	-	-	-	Data Link Layer State Changed Enable	Electromechanical Interlock Control	Power Controller Control	Power Indicator Control[1]	Power Indicator Control[0]
8Ah	Slot Status Register	R	Electromechanical Interlock Status	Presence Detect State	MRL Sensor State	Command Completed	Presence Detect Changed	MRL Sensor Changed	Power Fault Detected	Attn Botton pressed
8Bh		R	Reversed							Data Link Layer State Changed
8Ch-FFh	Reversed									

8.3. PCI Configuration Space Functions

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of the configuration space of the RTL8187SE are described below.

VID: Vendor ID. This field will be set to a value corresponding to a PCI Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh, which is Realtek Semiconductor's PCI Vendor ID.

DID: Device ID. This field will be set to a value corresponding to a PCI Device ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8185h.

Command: The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Table 10. Command Register in PCI Configuration Space

Bit	Symbol	Description
15:11	-	Reserved.
10	INTDIS	Interrupt Disable. This Bit enables/disables the RTL8187SE to assert Int# signal. 1: Force disable assertion of the Int# signal. 0: Enable enable assertion of the Int# signal (default value after PCI reset)
9	FBTBEN	Fast Back-To-Back Enable. Does not apply to PCI Express. Must be hardwired to 0.
8	SERREN	System Error Enable. When set to 1, enables reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI-Express specific bits in the Device Control register.
7	ADSTEP	Address/Data Stepping. Does not apply to PCI Express. Must be hardwired to 0.
6	PERRSP	Parity Error Response. In the Status register, the Master Data Parity Error bit is set by a Requester if its Parity Error Response bit is set and either of the following two conditions occurs: - If the Requester receives a poisoned Completion. - If the Requester poisons a write request. If the Parity Error Response bit is cleared, the Master Data Parity Error status bit is never set.
5	VGASNOOP	VGA Palette SNOOP. Does not apply to PCI Express. Must be hardwired to 0.
4	MWIEN	Memory Write and Invalidate Cycle Enable. Does not apply to PCI Express. Must be hardwired to 0.
3	SCYCEN	Special Cycle Enable. Does not apply to PCI Express. Must be hardwired to 0.
2	BMEN	Bus Master Enable. When set to 1, the RTL8187SE is capable of acting as a PCI bus master. When set to 0, it is prohibited from acting as a bus master. For normal operations, this bit must be set by the system BIOS.
1	MEMEN	Memory Space Access. When set to 1, the RTL8187SE responds to memory space accesses. When set to 0, the RTL8187SE ignores memory space accesses.
0	IOEN	IO Space Access. When set to 1, the RTL8187SE responds to IO space accesses. When set to 0, the RTL8187SE ignores IO space accesses.

8.4. PCI Configuration Space Status

8.4.1. Status

The status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Table 11. PCI Configuration Space Status

Bit	Symbol	Description
15	DPERR	Detected Parity Error. This bit is set by the RTL8187SE whenever it receives a Poisoned Transaction Layer Packet (TLP), regardless of the state the Parity Error Enable bit. Default value of this field is 0.
14	SSERR	Signaled System Error. This bit is set when the RTL8187SE sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. Default value of this field is 0.
13	RMABT	Received Master Abort. This bit is set when the RTL8187SE receives a Completion with Unsupported Request Completion Status. Default value of this field is 0.
12	RTABT	Received Target Abort. This bit is set when the RTL8187SE receives a Completion with Completer Abort Completion Status. Default value of this field is 0.
11	STABT	Signaled Target Abort. This bit is set when the RTL8187SE completes a Request using Completer Abort Completion Status. Default value of this field is 0.
10:9	DST1~0	Device Select Timing. Does not apply to PCI Express. Must be hardwired to 0.
8	DPD	Data Parity Error Detected. This bit is set by the RTL8187SE if its Parity Error Enable bit is set and either of the following two conditions occurs: - Requestor receives a Completion marked poisoned - Requestor poisons a write Request If the Parity Error Enable bit is cleared, this bit is never set. Default value of this field is 0.
7	FBBC	Fast Back-To-Back Capable. Does not apply to PCI Express. Must be hardwired to 0.
6	-	Reserved.
5	66MHz	66MHz Capable. Does not apply to PCI Express. Must be hardwired to 0.
4	NewCap	Capability List. Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.
3	INTSTS	Interrupt Status. This bit reflects the interrupt status of the RTL8187SE. Unlike ISR bits, this bit is a read-only bit and cannot be reset by writing a 1 to this bit. The only way to reset this bit is to reset the ISR register. The setting of the 'Interrupt Disable' bit in the Command Register has no effect on the state of the 'Interrupt Status' bit. Only when the 'Interrupt Disable' bit is a 0 and the 'Interrupt Status' bit is a 1, will the RTL8187SE's Int# signal be asserted.
2:0	-	Reserved.

8.4.2. RIDR (Revision ID Register)

The Revision ID register is an 8-bit register that specifies the RTL8187SE controller revision number.

8.4.3. PIFR (Programming Interface Register)

The programming interface register is an 8-bit register that identifies the programming interface of the RTL8187SE controller. The PCI 2.1 specification does not define a specific value for network devices. In the RTL8187SE controller this is PIFR = 00h.

8.4.4. SCR (Sub-Class Register)

The Sub-Class Register is an 8-bit register that identifies the function of the RTL8187SE. SCR=0x80 indicates that the RTL8187SE is identified as 'other network controller'.

8.4.5. BCR (Base-Class Register)

The Base-Class Register is an 8-bit register that broadly classifies the function of the RTL8187SE. BCR=02h indicates that the RTL8187SE is a network controller.

8.4.6. CLS (Cache Line Size)

This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

8.4.7. LTR (Latency Timer Register)

This register is also referred to as primary latency timer for Type 1 Configuration Space header devices. The primary/master latency timer does not apply to PCI Express. This register must be hardwired to 0.

8.4.8. HTR (Header Type Register)

Reads will return a 0, writes are ignored.

8.4.9. BIST (Built-In Self-Test)

Reads will return a 0, writes are ignored.

8.4.10. IOAR (Input Output Address Register)

This register specifies the BASE IO address, which is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into IO space.

Table 12. Input Output Address Register

Bit	Symbol	Description
31:8	IOAR31~8	Base Input Output Address. This is set by software to the Base IO address for the operational register map.
7:2	IOSIZE	Input Output Size Indication. Read back as 0. This allows the PCI bridge to determine that the RTL8187SE requires 256 bytes of IO space.
1	-	Reserved.
0	IOIN	IO Space Indicator. Read only. Set to 1 by the RTL8187SE to indicate that it is capable of being mapped into IO space.

8.4.11. MEMAR (Memory Address Register)

This register specifies the base memory address for memory accesses to the RTL8187SE operational registers. This register must be initialized prior to accessing any RTL8187SE register with memory access.

Table 13. Memory Address Register

Bit	Symbol	Description
31:8	MEM31~8	Base Memory Address. This is set by software to the base address for the operational register map.
7:4	MEMSIZE	Memory Size. These bits return 0, which indicates that the RTL8187SE requires 256 bytes of Memory Space.
3	MEMPF	Memory Pre-Fetchable. Read only. Set to 0 by the RTL8187SE.
2:1	MEMLOC	Memory Location Select. Read only. Set to 0 by the RTL8187SE. This indicates that the base register is 32 bits wide and can be placed anywhere in the 32-bit memory space.
0	MEMIN	Memory Space Indicator. Read only. Set to 0 by the RTL8187SE to indicate that it is capable of being mapped into memory space.

8.4.12. CISPtr (CardBus Card Information Structure Pointer)

CardBus CIS Pointer. This register does not apply to PCI Express. It must be read-only and must be hardwired to 0.

8.4.13. SVID (Subsystem Vendor ID)

This field will be set to a value corresponding to the PCI Subsystem Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh (Realtek Semiconductor's PCI Subsystem Vendor ID).

8.4.14. SMID (Subsystem ID)

This field will be set to a value corresponding to the PCI Subsystem ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8198h.

8.4.15. ILR (Interrupt Line Register)

The Interrupt Line Register is an 8-bit register used to indicate the routing of the interrupt. It is written by the POST software to set an interrupt line for the RTL8187SE.

8.4.16. IPR (Interrupt Pin Register)

The Interrupt Pin register is an 8-bit register indicating the interrupt pin used by the RTL8187SE. The RTL8187SE uses INTA interrupt pin. Read only. IPR = 01h.

8.4.17. MNGNT (Minimum Grant Timer: Read only)

This register does not apply to PCI Express. It must be read-only and must be hardwired to 0.

8.4.18. MXLAT (Maximum Latency Timer: Read only)

This register does not apply to PCI Express. It must be read-only and must be hardwired to 0.

8.5. Default Value After Power-On (RSTB Asserted)

Table 14. PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	1	1	1	0	1	1	0	0
01h		R	0	0	0	1	0	0	0	0
02h	DID	R	1	0	0	0	0	1	0	1
03h		R	1	0	0	0	0	0	0	1
04h	Command	R	0	0	0	0	0	0	0	0
		W	-	PERRSP	-	MWIEN	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	0	0	0	NewCap	0	0	0	0
07h		R	0	0	0	0	0	0	1	0
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	1	0	0	0	1	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	1	0	0	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	RW	0	0	0	0	0	0	0	0
0Dh	LTR	R	0	0	0	0	0	0	0	0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	1
11h		RW	0	0	0	0	0	0	0	0
12h		RW	0	0	0	0	0	0	0	0
13h		RW	0	0	0	0	0	0	0	0
14h	MEMAR	R	0	0	0	0	0	0	0	0
15h		RW	0	0	0	0	0	0	0	0
16h		RW	0	0	0	0	0	0	0	0
17h		RW	0	0	0	0	0	0	0	0
18h~27h	-	RESERVED (ALL 0)								
28h	CISPtr	R	0	0	0	0	0	0	0	0
29h		R	0	0	0	0	0	0	0	0
2Ah		R	0	0	0	0	0	0	0	0
2Bh		R	0	0	0	0	0	0	0	0
2Ch	SVID	R	1	1	1	0	1	1	0	0
2Dh		R	0	0	0	1	0	0	0	0
2Eh	SMID	R	1	0	0	0	0	1	0	1
2Fh		R	1	0	0	0	0	0	0	1
30h	BMAR	R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	BROMEN
31h		R	0	0	0	0	0	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		RW	0	0	0	0	0	0	0	0
33h		RW	0	0	0	0	0	0	0	0
34h	Cap-Ptr	R	Ptr7	Ptr6	Ptr5	Ptr4	Ptr3	Ptr2	Ptr1	Ptr0
35h~3Bh	-	RESERVED (ALL 0)								
3Ch	ILR	RW	0	0	0	0	0	0	0	0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	0	0	0	0	0	0
3Fh	MXLAT	R	0	0	0	0	0	0	0	0
40h~FFh	-	RESERVED (ALL 0)								

8.6. PCI Power Management Functions

The RTL8187SE is compliant with ACPI (Rev 2.0), PCI Power Management (Rev. 1.2), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-Directed Power Management (OSPM) environment.

The RTL8187SE can monitor the network for a Wakeup Frame, a Magic Packet, or a Re-LinkOk, and notify the system via PME# when such a packet or event occurs. Then the system can be restored to a normal state to process incoming jobs.

When the RTL8187SE is in power down mode (D1 ~ D3):

- The Rx state machine is stopped, and the RTL8187SE monitors the network for wakeup events such as a Magic Packet, Wakeup Frame, and/or Re-LinkOk, in order to wake up the system. When in power down mode, the RTL8187SE will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx FIFO buffer.
- The FIFO status and packets that have already been received into the Rx FIFO before entering power down mode are held by the RTL8187SE.
- Transmission is stopped. PCI bus master mode is stopped. The Tx FIFO buffer is held.
- After restoration to a D0 state, the RTL8187SE transfers data that was not moved into the Tx FIFO buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The D3cold_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power (bit15, PMC) = 1.

If EEPROM D3cold_support_PME bit (bit15, PMC) = 0, the above 4 bits are all 0's.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 F7, then PCI PMC = C3 F7)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 F7, then PCI PMC = 03 76)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C3 F7 (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 77, then PCI PMC = C3 77)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 77, then PCI PMC = 03 76)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 03 76.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8187SE, e.g. a broadcast, multicast, or unicast packet addressed to the current RTL8187SE adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in the current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid WLAN packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8187SE, e.g. a broadcast, multicast, or unicast address to the current RTL8187SE adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC* of the received Wakeup Frame matches the 16-bit CRC* of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8187SE is configured to allow direct packet wakeup, e.g. a broadcast, multicast, or unicast network packet.

**16-bit CRC: The RTL8187SE supports two normal wakeup frames (covering 64 mask bytes from offset 0 to 63 of any incoming network packet) and three long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).*

The PME# signal is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8187SE may assert PME# in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wakeup Frame has been received.

Note: Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8187SE to stop asserting a PME# (if enabled).

When the device is in power down mode, e.g. D1~D3, the IO, and MEM spaces are all disabled. After a RST# assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto-loaded from EEPROM). The setting may be changed from the EEPROM, if required. The RTL8187SE also supports the legacy LAN WAKE-UP function. The LWAKE pin is used to notify legacy motherboards to execute the wake-up process whenever the device receives a wakeup event, such as Magic Packet.

8.7. Message Signaled Interrupt (MSI)

8.7.1. MSI Capability Structure in PCI Configuration Space

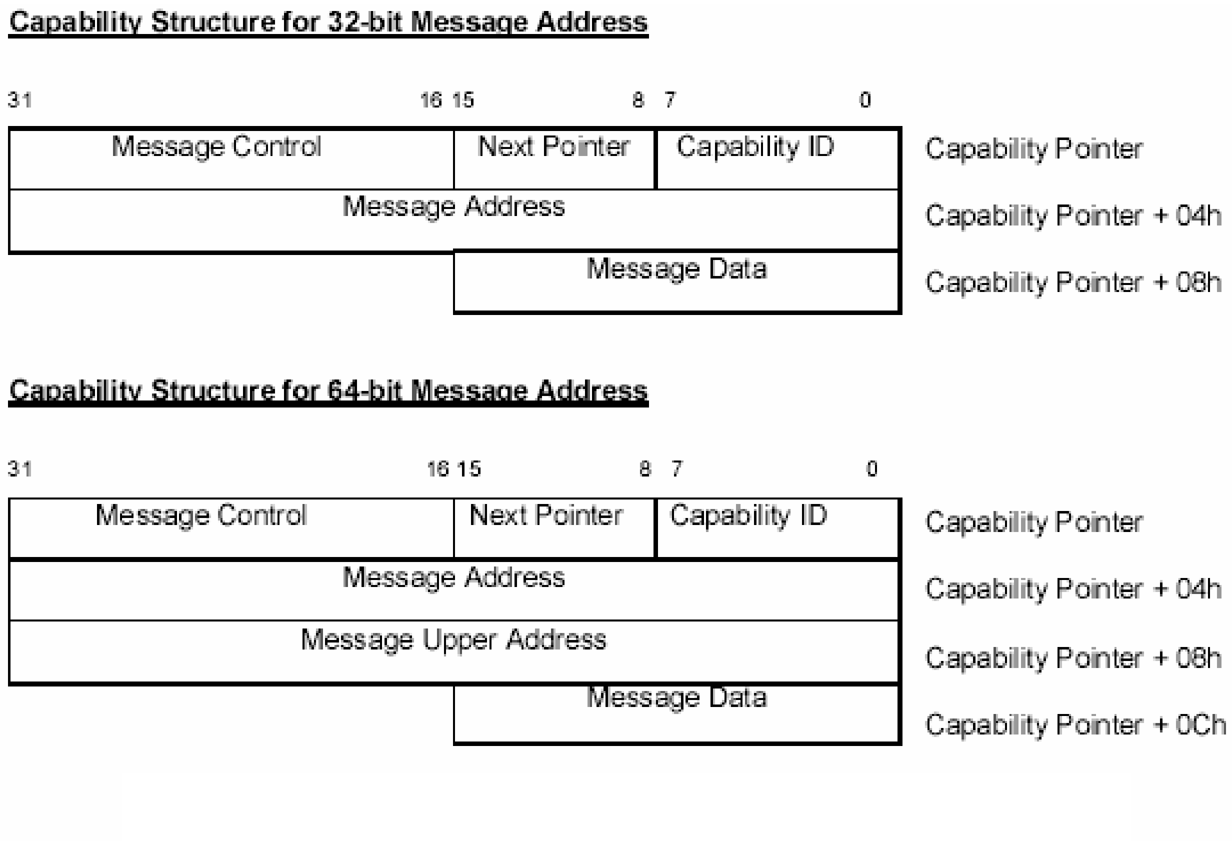


Figure 4. Message Capability Structure

8.7.2. Message Control

Table 15. Message Control

<table>
<tr><th>Bits</th><th>RW</th><th>Field</th><th colspan="2">Description</th></tr>
<tr><td>15:8</td><td>RO</td><td>Reserved</td><td colspan="2">Reserved. Always return 0</td></tr>
<tr><td>7</td><td>RO</td><td>64-Bit Address Capable</td><td colspan="2">1: The RTL8187SE is capable of generating a 64-bit message address.
0: The RTL8187SE is NOT capable of generating a 64-bit message address.
This bit is read only and the RTL8187SE is set to 1.</td></tr>
<tr><td rowspan="10">6:4</td><td rowspan="10">RW</td><td rowspan="10">Multiple Message Enable</td><td colspan="2">System software (e.g., BIOS, OS) indicates to the RTL8187SE the number of allocated messages/vectors (equal to or less than the number of requested messages/vectors).
This field after PCI reset is ‘000’.</td></tr>
<tr><td>Encoding</td><td>Number of Messages/Vectors</td></tr>
<tr><td>000</td><td>1</td></tr>
<tr><td>001</td><td>2</td></tr>
<tr><td>010</td><td>4</td></tr>
<tr><td>011</td><td>8</td></tr>
<tr><td>100</td><td>16</td></tr>
<tr><td>101</td><td>32</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
<tr><td rowspan="4">3:1</td><td rowspan="4">RO</td><td rowspan="4">Multiple Message Capable</td><td colspan="2">Indication to system software (e.g., BIOS, OS) of the number of RTL8187SE requested vectors.
The RTL8187SE supports only one vector messages/vectors.</td></tr>
<tr><td>Encoding</td><td>Number of Messages/Vectors</td></tr>
<tr><td>000</td><td>1</td></tr>
<tr><td>Others</td><td>Reserved</td></tr>
<tr><td>0</td><td>RW</td><td>MSI Enable</td><td colspan="2">1: Enable MSI (Also the INTx pin is disabled automatically, MSI and INTx are mutually exclusive), this bit is set by system software.
0: Disable MSI (Default value after power-on or PCI reset)</td></tr>
</table>

8.7.3. Message Address

Table 16. Message Address

Bits	RW	Field	Description
31:02	RW	Message Address	System-Specified Message/Vector Address. Low DWORD aligned address for MSI memory write transaction.
01:00	RO	Reserved	Always Return ‘00’. This bit is read only.

8.7.4. Message Upper Address

Table 17. Message Upper Address

Bits	RW	Field	Description
31:00	RW	Message Upper Address	System-Specified Message/Vector Upper Address. Upper 32 bits of a 64-bit message/vector address. This register is effective only when the DAC function is enabled, i.e., 64-bit addressing is enabled; bit7 in Message Control register is set. If the contents of this register are 0, the RTL8187SE only performs 32-bit addressing for the memory write of the messages/vectors. This bit is read/write.

8.7.5. Message Data

Table 18. Message Data

Bits	RW	Field	Description
15:00	RW	Message Data	If the Message Enable bit is set, the message/vector data is driven onto the lower word of the memory write transaction's data phase. This bit is read/write.

9. Functional Description

9.1. Transmit & Receive Operations

The RTL8187SE supports a descriptor-based buffer management that will significantly lower host CPU utilization. The RTL8187SE supports an infinite number of consecutive transmit descriptors, and 64 consecutive receive descriptors, in memory.

There may be a maximum of five descriptor rings. Transmit descriptor rings consist of one beacon transmit descriptor ring, one high priority descriptor ring, one normal priority descriptor ring, and one low priority descriptor ring. Each transmit descriptor ring may consist of an infinite number of 8-double-word consecutive descriptors, and the receive descriptor array may consist of up to sixty-four 4-double-word consecutive descriptors. The start address of each descriptor group should be in 256byte alignment. Software must pre-allocate enough buffers and configure all descriptor rings before transmitting and/or receiving packets.

9.1.1. Transmit

The following describes what the Tx descriptor may look like, depending on different states in each Tx descriptor.

Tx Descriptor Format (before transmitting, OWN=1, Tx command mode 1)

Table 19. Tx Descriptor Format (before transmitting, OWN=1, Tx command mode 1)

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27 26 25 24</th><th>23</th><th>22 21 20 19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14 13 12</th><th>11 10 9 8 7 6 5 4 3 2 1 0</th><th></th></tr>
<tr><td>OWN=1</td><td>DMA_OK</td><td>FS</td><td>LS</td><td>TXRATE (4 bits)</td><td>RTSEN</td><td>RTSRATE (4 bits)</td><td>CTSEN</td><td>MOREFRAG</td><td>SPLCP</td><td>NO_ENCRYPT</td><td>BSSID_NO</td><td>TPKTSIZE (12 bits)</td><td>Offset 0</td></tr>
<tr><td>LENGEXT</td><td colspan="9">Length (15 bits)</td><td colspan="3">RTSDUR (16 bits)</td><td>Offset 4</td></tr>
<tr><td colspan="13">TX_BUFFER_ADDRESS</td><td>Offset 8</td></tr>
</table>

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th></th></tr>
<tr><td colspan="16">DURATION (16 bits)</td><td>MIC_CAL</td><td colspan="3">RSVD (3 bits)</td><td colspan="12">Frame_Length (12 bits)</td><td>Offset 12</td></tr>
<tr><td colspan="32">NEXT_TX_DESCRIPTOR_ADDRESS</td><td>Offset 16</td></tr>
<tr><td colspan="5">RATE_FALLBACK_LIMIT (5 bits)</td><td colspan="4">RTS_RATE_FALLBACK_LIMIT (4 bits)</td><td colspan="4">RSVD (4bits)</td><td>PIFS</td><td>NO_ACM</td><td>RT_DB</td><td colspan="8">RETRY_LIMIT (8 bits)</td><td colspan="8">RTSAGC (8 bits)</td><td>Offset 20</td></tr>
<tr><td>RSVD</td><td colspan="2">SPC</td><td>ANTENNA</td><td colspan="8">AGC (8 bits)</td><td colspan="4">RSVD (4bits)</td><td colspan="16">DELAY_BOUND (16 bits)</td><td>Offset 24</td></tr>
<tr><td colspan="16">FRAG_QSIZE (16 bits)</td><td>EN_PMPD</td><td>EN_BCKEY</td><td colspan="6">BCKEY (6 bits)</td><td>PT_EN</td><td>TPC_EN</td><td colspan="2">TPC_POLARITY</td><td>TPC_DESEN</td><td>RSVD</td><td colspan="2">HW Length Select</td><td>Offset 28</td></tr>
</table>

Table 20. Tx Status Descriptor

<table>
<tr><th>Offset#</th><th>Bit#</th><th>Symbol</th><th>Description</th></tr>
<tr><td>0</td><td>31</td><td>OWN</td><td>Ownership.
When set, this bit indicates that the descriptor is owned by the NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1.</td></tr>
<tr><td>0</td><td>30</td><td>DMA OK</td><td>DMA OK.
Set by the driver, reset by the RTL8187SE when TX DMA OK. If IMR’s corresponding bit is set and the driver sets this bit, the RTL8187SE resets this bit and issues an interrupt right after DMA OK of the last segment (LS). If not, the RTL8187SE just resets this bit without asserting an interrupt.</td></tr>
<tr><td>0</td><td>29</td><td>FS</td><td>First Segment Descriptor.
When set, this bit indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.</td></tr>
<tr><td>0</td><td>28</td><td>LS</td><td>Last Segment Descriptor.
When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.</td></tr>
<tr><td>0</td><td>27:24</td><td>TXRATE</td><td>Tx Rate.
These five bits indicate the current frame’s transmission rate.
<table>
<tr><th></th><th>Bit 27</th><th>Bit 26</th><th>Bit 25</th><th>Bit 24</th></tr>
<tr><td>1Mbps</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2Mbps</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>5.5Mbps</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>11Mbps</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>6Mbps</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>9Mbps</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>12Mbps</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>18Mbps</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>24Mbps</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>36Mbps</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>48Mbps</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>54Mbps</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Reserved</td><td colspan="4">All Other Combinations</td></tr>
</table></td></tr>
<tr><td>0</td><td>23</td><td>RTSEN</td><td>RTS Enable.
Set to 1, indicates that an RTS/CTS handshake shall be performed at the beginning of any frame exchange sequence where:
The frame is of type Data or Management,
the frame has a unicast address in the Address1 field,
and the length of the frame is greater than RTSThreshold.</td></tr>
</table>

<table>
<tr><th>Offset#</th><th>Bit#</th><th>Symbol</th><th>Description</th></tr>
<tr><td>0</td><td>22:19</td><td>RTSRATE</td><td>RTS Rate.
These four bits indicate the RTS frame’s transmission rate before transmitting the current frame, and will be ignored if the RTSEN bit is set to 0.
<table>
<tr><th></th><th>Bit 22</th><th>Bit 21</th><th>Bit 20</th><th>Bit 19</th></tr>
<tr><td>1Mbps</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2Mbps</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>5.5Mbps</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>11Mbps</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>6Mbps</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>9Mbps</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>12Mbps</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>18Mbps</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>24Mbps</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>36Mbps</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>48Mbps</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>54Mbps</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Reserved</td><td colspan="4">All Other Combinations</td></tr>
</table></td></tr>
<tr><td>0</td><td>18</td><td>CTSEN</td><td>CTS Enable.
Both RTSEN and CTSEN set to 1 indicates that the CTS-to-self protection mechanism will be used.</td></tr>
<tr><td>0</td><td>17</td><td>MOREFRAG</td><td>More Fragments.
This bit is set to 1 in all data type frames that have another fragment of the current packet to follow.</td></tr>
<tr><td>0</td><td>16</td><td>SPLCP</td><td>Short Physical Layer Convergence Protocol format.
When set, this bit indicates that a short PLCP preamble will be added to the header before transmitting the frame.</td></tr>
<tr><td>0</td><td>15</td><td>NO_ENCRYPT</td><td>No Encryption.
This packet will be transmitted without encryption even if Tx encryption is enabled.</td></tr>
<tr><td>0</td><td>14:12</td><td>BSSID_NO</td><td>BSSID Number.</td></tr>
<tr><td>0</td><td>11:0</td><td>TPKTSIZE</td><td>Transmit Packet Size.
This field indicates the number of bytes required to transmit the frame.</td></tr>
<tr><td>4</td><td>31</td><td>LENGEXT</td><td>Length Extension.
This bit is used to supplement the Length field (bits 30:16, offset 4). This bit will be ignored if the TXRATE is set to 1Mbps, 2Mbps, or 5.5Mbps.</td></tr>
<tr><td>4</td><td>30:16</td><td>Length</td><td>Physical Layer Conversion Protocol (PLCP) Length.
The PLCP length field indicates the number of microseconds required to transmit the frame.</td></tr>
<tr><td>4</td><td>15:0</td><td>RTSDUR</td><td>Request To Send (RTS) Duration.
These bits indicate the RTS frame’s duration field before transmitting the current frame and will be ignored if the RTSEN bit is set to 0.</td></tr>
<tr><td>8</td><td>31:0</td><td>TxBuff</td><td>32-Bit Transmit Buffer Address.</td></tr>
<tr><td>12</td><td>31:16</td><td>DURATION</td><td>Time duration to send this packet plus SIFS and ACK</td></tr>
<tr><td>12</td><td>15</td><td>MIC_CAL</td><td>Enable MIC Calculation.</td></tr>
</table>

Offset#	Bit#	Symbol	Description
12	14:12	RSVD	Reserved.
12	11:0	Frame_Length	Transmit Frame Length. This field indicates the length in the Tx buffer, in bytes, to be transmitted.
16	31:0	NTDA	32-Bit Address of the Next Transmit Descriptor.
20	31:27	RATE_FALL BACK_LIMIT	Data Rate Auto Fallback Limit.
20	26:23	RTS_RATE_FALL BACK_LIMIT	RTS/CTS Rate Auto Fallback Limit.
20	22:19	RSVD	Reserved.
20	18	PIFS	Point Inter-Frame Space (PIFS). Setting this bit will cause this frame to be sent after PIFS
20	17	NO_ACM	No Admission Control Procedure. This packet will be sent out without being restricted by admission control procedures. For example, the management type frames shall be sent using the access category AC_VO without being restricted by admission control procedures.
20	16	RT_DB	Lifetime limited by RETRY_LIMIT (RT_DB=0) or DELAY_BOUND (RT_DB=1).
20	15:8	RETRY_LIMIT	Retry Count Limit.
20	7:0	RTSAGC	Tx RTS AGC.
24	31	RSVD	Reserved.
24	30:29	SPC	Short Preamble Count. 00: 10 bits 01: 12 bits 10: 14 bits 11: 16 bits
24	28	ANTENNA	Tx Antenna.
24	27:20	AGC	Tx AGC.
24	19:16	RSVD	Reserved.
24	15:0	DELAY_BOUND	Delay Bound
28	31:16	FRAG_QSIZE	Fragmentation Queue Size. Upon sending the first frame of a fragmentation sequence, the driver writes the queue size of the entire fragmentation exchange (including the first frame) here. MAC uses this value when counting down TXOP. This field is valid when TCR (0x40) duration processing fields are set to mode 1 or 2.
28	15	ENPMPD	Enable Power Meter Pre-Distortion Packet.
28	14	EN_BCKEY	Enable Broadcast/Multicast Key Search When Using Multiple BSSID
28	13:8	BCKEY	Specify key to use in CAM for broadcast/multicast.
28	7	PT_EN	Enable Power Tracking.
28	6	TPC_EN	Enable Transmit Power Control.
28	5:4	TPC_POLARITY	TPC Polarity Select. 00: Neither increment nor decrement. 01: Increment 10: Decrement 11: Reserved

Offset#	Bit#	Symbol	Description
28	3	TPC_DESEN	TPC Descriptor AGC Enable. 0: Use the value of register TPC_TXAGC_OFDM as 54MHz TXAGC Base 1: Use the value of AGC in the same descriptor as 54MHz TXAGC Base
28	1:0	HWLengthSelect	HW Length Select. 00: No Encryption 01: RC4 Encryption 10: AES Encryption 11: Reserved

Tx Status Descriptor (after transmitting, OWN=0, Tx status mode)

After having transmitted, the Tx descriptor becomes a Tx status descriptor.

Table 21. Tx Status Descriptor (after transmitting, OWN=0, Tx status mode)

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27 26 25 24 23 22 21 20 19 18 17</th><th>16</th><th>15</th><th>14 13 12 11 10 9 8</th><th>7 6 5 4 3 2 1 0</th><th></th></tr>
<tr><td>OWN=0</td><td>DMA_OK</td><td>FS</td><td>LS</td><td>RSVD (11 bits)</td><td>UDR</td><td>TOK</td><td>RTS RC (7 bits)</td><td>Packet RC (8 bits)</td><td>Offset 0</td></tr>
<tr><td colspan="6">MPDUExchangeTime (16 bits)</td><td colspan="3">RSVD</td><td>Offset 4</td></tr>
<tr><td colspan="9">TX_BUFFER_ADDRESS</td><td>Offset 8</td></tr>
<tr><td colspan="8">RSVD (20 bits)</td><td>Frame_Length (12 bits)</td><td>Offset 12</td></tr>
<tr><td colspan="9">NEXT_TX_DESCRIPTOR_ADDRESS</td><td>Offset 16</td></tr>
<tr><td colspan="9">RSVD</td><td>Offset 20</td></tr>
<tr><td colspan="9">RSVD</td><td>Offset 24</td></tr>
<tr><td colspan="9">RSVD</td><td>Offset 28</td></tr>
</table>

Table 22. Tx Status Descriptor (after transmitting, OWN=0, Tx status mode)

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership. When set, this bit indicates that the descriptor is owned by the NIC. When clear, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the related buffer data has been transmitted. In this case, OWN=0.
0	30	DMA_OK	DMA Okay.
0	29	FS	First Segment Descriptor. When set, this bit indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	Last Segment Descriptor. When set, this bit indicates that this is the last descriptor of a Tx packet, and that this descriptor is pointing to the last segment of the packet.
0	27:17	RSVD	Reserved.
0	16	UDR	FIFO under-run during transmission of this packet.
0	15	TOK	Transmit (Tx) OK. Indicates that a packet exchange sequence has completed successfully.
0	14:8	RTS RC	RTS Retry Count. The RTS RC's initial value is 0. It indicates the number of retries of RTS.
0	7:0	Packet RC	Packet Retry Count. The RC's initial value is 0. It indicates the number of retries before a packet was transmitted properly.
4	31:16	MPDUExchangeTime	MPDUExchangeTime corresponds to the just completed MPDU exchange. The MPDUExchangeTime equals the time required to transmit the MPDU sequence, i.e., the time required to transmit the MPDU plus the time required to transmit the expected response frame plus one SIFS.
4	15:0	RSVD	Reserved.
8	31:0	TxBuff	32-bit Transmit Buffer Address.
12	31:12	RSVD	Reserved.
12	11:0	Frame_Length	Transmit Frame Length. This field indicates the length in the Tx buffer, in bytes, to be transmitted.
16	31:0	NTDA	32-bit Address of Next Transmit Descriptor.
20	31:0	RSVD	Reserved.
24	31:0	RSVD	Reserved.
28	31:0	RSVD	Reserved.

9.1.2. Receive

This section describes what an Rx descriptor could look like, depending on different states in each Rx descriptor. An Rx buffer pointed to by one of the Rx descriptors should be at least 4 bytes.

Rx Command Descriptor (OWN=1)

The driver should pre-allocate Rx buffers and configure Rx descriptors before packet reception. The following describes what a Rx descriptor may look like before packet reception.

Table 23. Rx Command Descriptor (OWN=1)

31	30	29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0	
OWN=1	EOR	RSVD (18 bits)	Buffer_Size (12 bits)	Offset 0
RSVD				Offset 4
RX_BUFFER_ADDRESS				Offset 8
RSVD				Offset 12
RSVD				Offset 16

Table 24. Rx Command Descriptor (OWN=1)

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership. When set, this bit indicates that the descriptor is owned by the NIC, and is ready to receive a packet. The OWN bit is set by the driver after having pre-allocated a buffer at initialization, or the host has released the buffer to the driver. In this case, OWN=1.
0	30	EOR	End of Rx Descriptor Ring. This bit set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29:12	RSVD	Reserved.
0	11:0	Buffer_Size	Buffer Size. This field indicates the receive buffer size in bytes.
4	31:0	RSVD	Reserved.
8	31:0	RxBuff	32-bit Receive Buffer Address.
12	31:0	RSVD	Reserved.

Rx Status Descriptor (OWN=0)

When packet is received, the Rx command descriptor becomes a Rx status descriptor.

Table 25. Rx Status Descriptor (OWN=0)

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th></th></tr>
<tr><td>OWN=0</td><td>EOR</td><td>FS</td><td>LS</td><td>DMAF</td><td>FOVF</td><td>SPLCP</td><td>TRSW</td><td colspan="4">RXRATE (4 bits)</td><td>QOS</td><td>MAR</td><td>PAM</td><td>BAR</td><td>RES</td><td>PWRMGT</td><td>CRC32</td><td>ICV</td><td colspan="12">Frame_Length (12 bits)</td><td>Offset 0</td></tr>
<tr><td colspan="32">TSFTL</td><td>Offset 4</td></tr>
<tr><td colspan="32">TSFTH</td><td>Offset 8</td></tr>
<tr><td>RSVD</td><td colspan="4">RSVD (4 bits)</td><td>SHIFT</td><td>WAKEUP</td><td>DECRYPTED</td><td colspan="8">AGC (8 bits)</td><td>ANTENNA</td><td colspan="7">RSSI (7 bits)</td><td colspan="8">SQ (8 bits)</td><td>Offset 12</td></tr>
<tr><td colspan="8">FOT (8 bits)</td><td colspan="8">PWDB_GI2 (8 bits)</td><td colspan="6">CFO_BIAS (6 bits)</td><td colspan="6">SNR_LONG2END (6 bits)</td><td colspan="4">NUM_MCSI (4 bits)</td><td>Offset 16</td></tr>
</table>

Table 26. Rx Status Descriptor

<table>
<tr><th>Offset#</th><th>Bit#</th><th>Symbol</th><th>Description</th></tr>
<tr><td>0</td><td>31</td><td>OWN</td><td>Ownership.
When set, this bit indicates that the descriptor is owned by the NIC. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the NIC has filled this Rx buffer with a packet or part of a packet. In this case, OWN=0.</td></tr>
<tr><td>0</td><td>30</td><td>EOR</td><td>End Of Rx Descriptor Ring.
This bit set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.</td></tr>
<tr><td>0</td><td>29</td><td>FS</td><td>First Segment Descriptor.
When set, this bit indicates that this is the first descriptor of a received packet, and that this descriptor is pointing to the first segment of the packet.</td></tr>
<tr><td>0</td><td>28</td><td>LS</td><td>Last Segment Descriptor.
When set, this bit indicates that this is the last descriptor of a received packet, and this descriptor is pointing to the last segment of the packet.</td></tr>
<tr><td>0</td><td>27</td><td>DMAF</td><td>RX DMA Fail.
When set, this packet will be dropped by software.</td></tr>
<tr><td>0</td><td>26</td><td>FOVF</td><td>FIFO Overflow.
When set, this bit indicates that the receive FIFO was exhausted before this packet was fully received.</td></tr>
<tr><td>0</td><td>25</td><td>SPLCP</td><td>Short Physical Layer Convergence Protocol format.
When set, this bit indicates that a short PLCP preamble was added to the current received frame.</td></tr>
<tr><td>0</td><td>24</td><td>TRSW</td><td>T/R Switch.</td></tr>
<tr><td>0</td><td>23:20</td><td>RXRATE</td><td>Rx Rate.
These four bits indicate the current frame's receiving rate.
<table>
<tr><th></th><th>Bit 23</th><th>Bit 22</th><th>Bit 21</th><th>Bit 20</th></tr>
<tr><td>1Mbps</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2Mbps</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>5.5Mbps</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>11Mbps</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>6Mbps</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>9Mbps</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>12Mbps</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>18Mbps</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>24Mbps</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>36Mbps</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>48Mbps</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>54Mbps</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Reserved</td><td colspan="4">All Other Combinations</td></tr>
</table></td></tr>
<tr><td>0</td><td>19</td><td>QoS</td><td>QoS Packet Received.
When set, this bit indicates that a QoS packet was received.</td></tr>
</table>

Offset#	Bit#	Symbol	Description
0	18	MAR	Multicast Address Packet Received. When set, this bit indicates that a multicast packet was received.
0	17	PAM	Physical Address Matched. When set, this bit indicates that the destination address of this Rx packet matches the value in the RTL8187SE's ID registers.
0	16	BAR	Broadcast Address Received. When set, this bit indicates that a broadcast packet was received. BAR and MAR will not be set simultaneously.
0	15	RES	Receive Error. Valid if DMAF=0
0	14	PWRMGT	Receive Power Management Packet. When set, this bit indicates that the Power Management bit is set on the received packet.
0	13	CRC32	CRC32 Error. When set, this bit indicates that a CRC32 error has occurred on the received packet. A CRC32 packet can be received only when RCR_ACRC32 is set.
0	12	ICV	Integrity Check Value Error. When set, this bit indicates that an ICV error has occurred on the received packet. An ICV packet can be received only when RCR_AICV is set.
0	11:0	Frame_Length	When OWN=0 and LS =1, this bit indicates the received packet length, including CRC32, in bytes.
4	31:0	TSFTL	A snapshot of the TSFTR's least significant 32 bits. Valid only when LS is set.
8	31:0	TSFTH	A snapshot of the TSFTR's most significant 32 bits. Valid only when LS is set.
12	31:27	RSVD	Reserved.
12	26	SHIFT	0: 4-byte alignment not needed. 1: 4-byte alignment needed.
12	25	WAKEUP	The received packet is a unicast wakeup packet.
12	24	DECRYPTED	The received packet has been decrypted.
12	23:16	AGC	The AGC of the received packet.
12	15	ANTENNA	The received packet is received through this antenna.
12	14:8	RSSI	Received Signal Strength Indicator. The RSSI is a measure of the RF energy received by the PHY.
12	7:0	SQ	Signal Quality. The SQ is a measure of the quality of BAKER code lock, providing an effective measure during the full reception of a PLCP preamble and header.
16	31:24	FOT	Final frequency offset estimate (*2.44kHz), s(8.0) FOT x 2.44kHz.
16	23:16	PWdB	Received Power in dB at flag_gi2 up, s(8.1) RxPower=PWdB/2-42dBm.
16	15:10	CFO_Bias	Frequency difference between final frequency offset tracking and coarse frequency offset estimation (FOT-CFOE) x 2.44kHz.
16	9:4	SNR_LONG2END	Measured SNR in dB by the difference between LONG1 and LONG2, s(8.2) SnrLong = SNR_LONG2END/4dB.
16	3:0	NUM_MCSI	Number of MCSI (Masked-CSI subcarriers).

9.2. *Loopback Operation*

Loopback mode is normally used to verify that the logic operations have performed correctly. In loopback mode, the RTL8187SE takes frames from the transmit descriptor and transmits them up to internal Rx logic. The loopback function does not apply to an external PHYceiver.

9.3. *QoS Functions*

The RTL8187SE supports WMM, APSD, and IEEE 802.11e functions.

9.4. *LED Functions*

The RTL8187SE supports 2 LED signals in 4 configurable operation modes.

- Software Control Mode: In this mode, LED can be totally controlled by software.
- Tx/Rx Active Mode: Active when transmission or reception occurs. Can be configured as high active or low active.
- Tx Active Mode: Active while transmitting. Can be configured as high active or low active.
- Rx Active Mode: Active while receiving. Can be configured as high active or low active.

10. Application Diagram

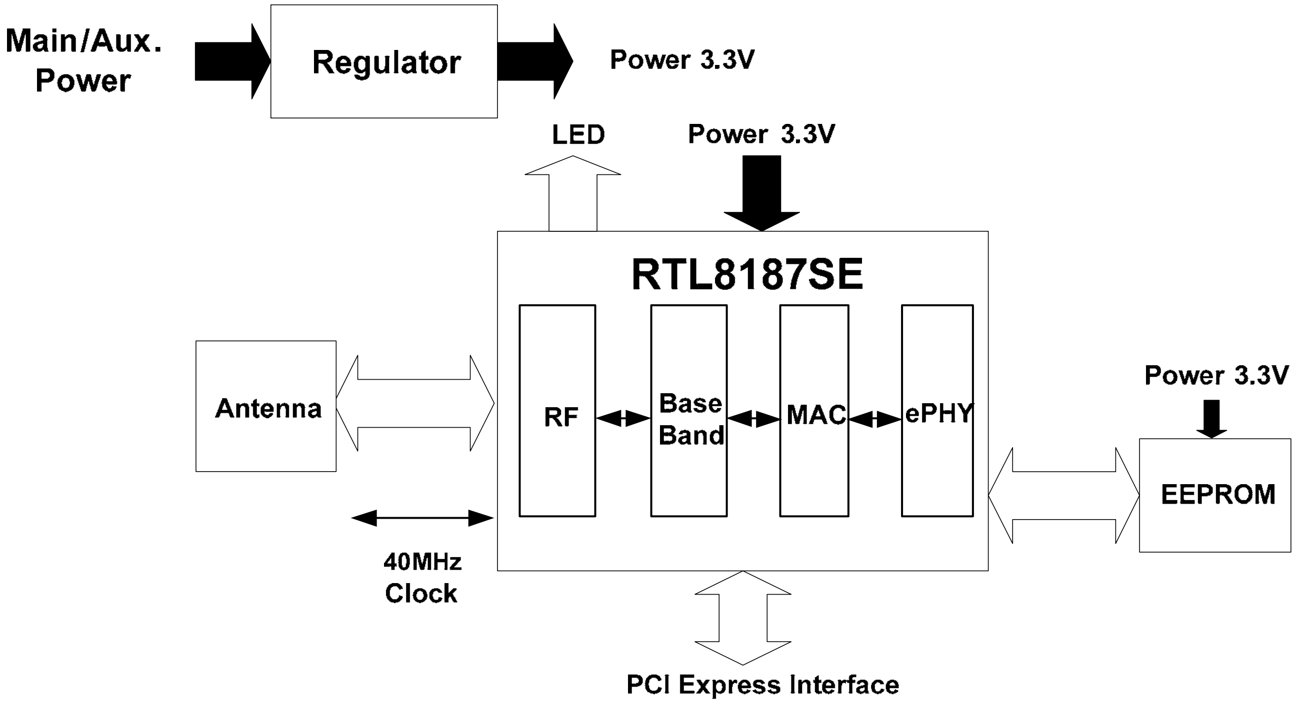


Figure 5. Application Diagram

11. Electrical Characteristics

11.1. Temperature Limit Ratings

Table 27. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

11.2. DC Characteristics

Table 28. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33	3.3V Supply Voltage	-	3.0	3.3	3.6	V
VDD18	1.8V Supply Voltage	-	1.7	1.8	1.9	V
V_{oh}	Minimum High Level Output Voltage	I_{oh}=-8mA	0.9*Vcc	-	Vcc	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol}=8mA	-	-	0.1*Vcc	V
V_{ih}	Minimum High Level Input Voltage	-	0.5*Vcc	-	Vcc+0.5	V
V_{il}	Maximum Low Level Input Voltage	-	-0.5	-	0.3*Vcc	V
I_{in}	Input Current	V_{in}=V_{cc} or GND	-1.0	-	1.0	µA
I_{oz}	Tri-State Output Leakage Current	V_{out}=V_{cc} or GND	-10	-	10	µA
I_{cc}	Average Operating Supply Current	I_{out}=0mA	-	-	242	mA

11.3. AC Characteristics

11.3.1. Serial EEPROM Interface Timing (93C46(64*16)/93C56(128*16))

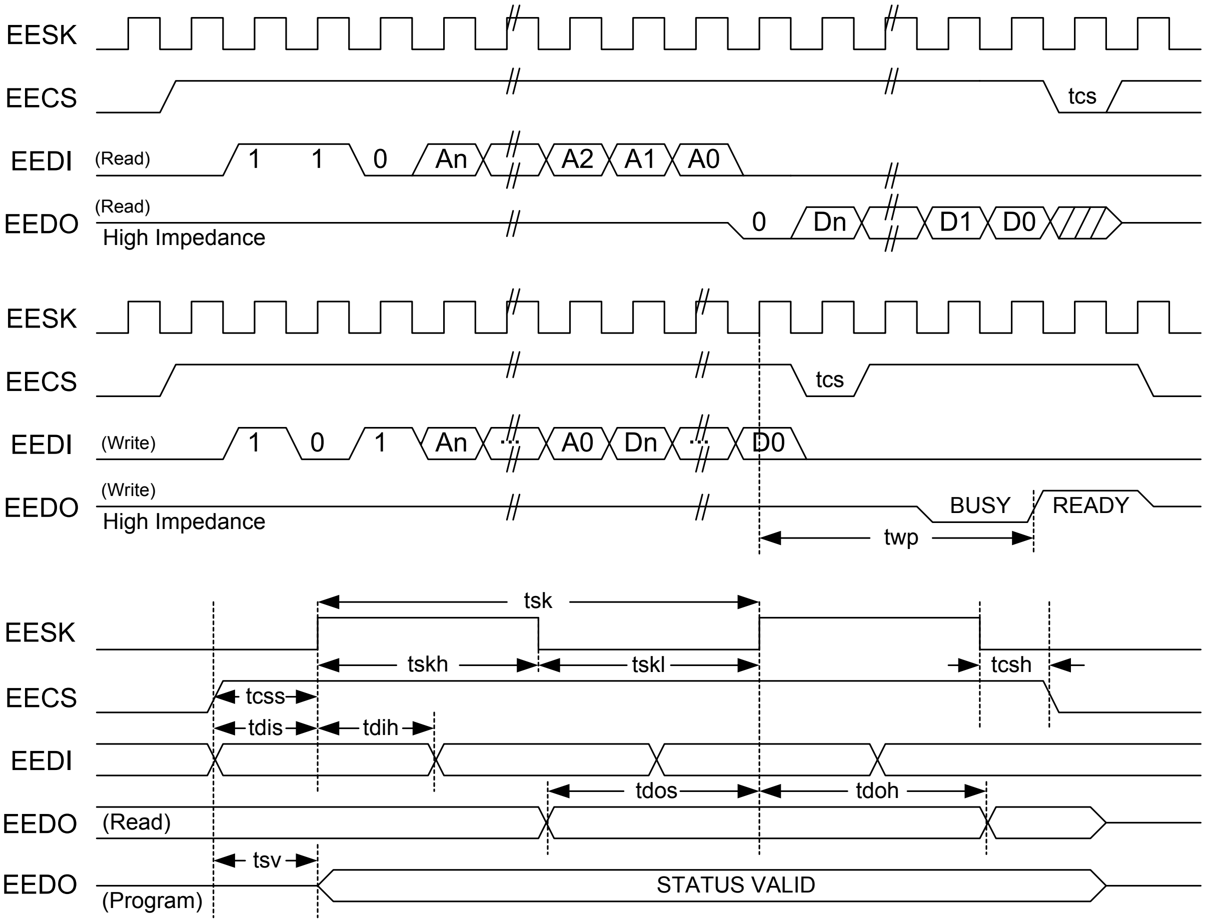


Figure 6. Serial EEPROM Interface Timing

Table 29. EEPROM Access Timing Parameters

Symbol	Parameter		Minimum	Typical	Maximum	Units
tcs	Minimum CS Low Time	9346/9356	1000/250	-	-	ns
twp	Write Cycle Time	9346/9356	-	-	10/10	ms
tsk	SK Clock Cycle Time	9346/9356	4/1	-	-	µs
tskh	SK High Time	9346/9356	1000/500	-	-	ns
tskl	SK Low Time	9346/9356	1000/250	-	-	ns
tcss	CS Setup Time	9346/9356	200/50	-	-	ns
tcsh	CS Hold Time	9346/9356	0/0	-	-	ns
tdis	DI Setup Time	9346/9356	400/50	-	-	ns
tdih	DI Hold Time	9346/9356	400/100	-	-	ns
tdos	DO Setup Time	9346/9356	2000/500	-	-	ns
tdoh	DO Hold Time	9346/9356	-	-	2000/500	ns
tsv	CS to Status Valid	9346/9356	-	-	1000/500	ns

11.4. PCI Express Bus Parameters

11.4.1. Differential Transmitter Parameters

Table 30. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{\text{TX-DIFFp-p}}$	Differential Peak to Peak Output Voltage	0.800	-	1.2	V
$V_{\text{TX-DE-RATIO}}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
$T_{\text{TX-EYE}}$	Minimum Tx Eye Width	0.75	-	-	UI
$T_{\text{TX-EYE-MEDIAN-to-MAX-JITTER}}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.125	UI
$T_{\text{TX-RISE}}$, $T_{\text{TX-FALL}}$	D+/D- Tx Output Rise/Fall Time	0.125	-	-	UI
$V_{\text{TX-CM-ACp}}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{\text{TX-CM-DCACTIVE-IDLEDELTA}}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{\text{TX-CM-DCLINE- DELTA}}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{\text{TX-IDLE-DIFFp}}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{\text{TX-RCV-DETECT}}$	The amount of voltage change allowed during Receiver Detection	-	-	600	mV
$V_{\text{TX-DC-CM}}$	The TX DC Common Mode Voltage	0	-	3.6	V
$I_{\text{TX-SHORT}}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{\text{TX-IDLE-MIN}}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{\text{TX-IDLE- SETTO-IDLE}}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered set	-	-	20	UI
$T_{\text{TX-IDLE-TOTO-DIFF-DATA}}$	Maximum time to transition to valid TX specifications after leaving an Electrical Idle condition	-	-	20	UI
$RL_{\text{TX-DIFF}}$	Differential Return Loss	10	-	-	dB
$RL_{\text{TX-CM}}$	Common Mode Return Loss	6	-	-	dB
$Z_{\text{TX-DIFF-DC}}$	DC Differential TX Impedance	80	100	120	Ω
$L_{\text{TX-SKEW}}$	Lane-to-Lane Output Skew	-	-	500+2UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{\text{crosslink}}$	Crosslink Random Timeout	0	-	1	ms

Note1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

Note2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30 kHz – 33 kHz. The +/- 300 ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600 ppm difference.

11.4.2. Differential Receiver Parameters

Table 31. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Input Peak to Peak Voltage	0.175	-	1.200	V
$T_{RX\text{-}EYE}$	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.3	UI
$V_{RX\text{-}CM\text{-}ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX\text{-}DIFF}$	Differential Return Loss	10	-	-	dB
$RL_{RX\text{-}CM}$	Common Mode Return Loss	6	-	-	dB
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance	80	100	120	Ω
$Z_{RX\text{-}\text{-}DC}$	DC Input Impedance	40	50	60	Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX\text{-}IDLE\text{-}DET\text{-}DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX\text{-}SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

11.4.3. REFCLK Parameters

Table 32. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Max Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Min Input Voltage	-	-0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching	-	20	%	1, 14
$Z_{C\text{-}DC}$	Clock Source DC Impedance	40	60	Ω	1, 11

Note1: Measurement taken from single ended waveform.

Note2: Measurement taken from differential waveform.

Note3: Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

Note4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

Note5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

Note6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation.

Note7: Defined as the maximum instantaneous voltage including overshoot.

Note8: Defined as the minimum instantaneous voltage including undershoot.

Note9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.

Note10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.

Note11: System board compliance measurements must use the test load card described in Figure16. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL = 2 pF.

Note12: T_{STABLE} *is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the* V_{RB} *±100 mV differential range. See Figure 15.*

*Note13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 PPM then we have a error budget of 100 Hz/PPM * 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800 PPM*

Note14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-, the maximum allowed difference should not exceed 20% of the slowest edge rate.

Note15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

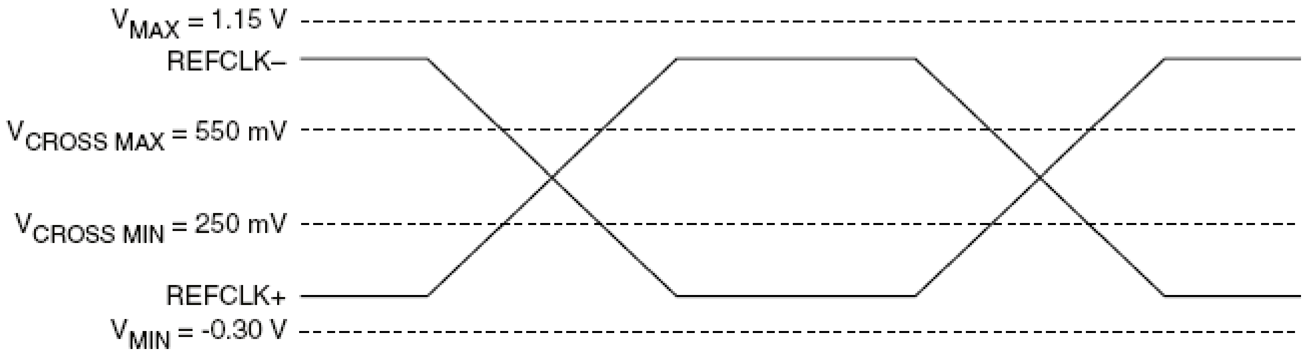


Figure 7. Single-Ended Measurement Points for Absolute Cross Point and Swing

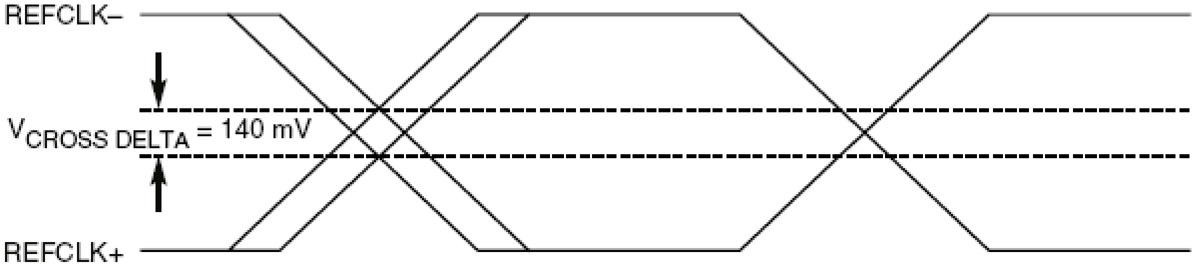


Figure 8. Single-Ended Measurement Points for Delta Cross Point

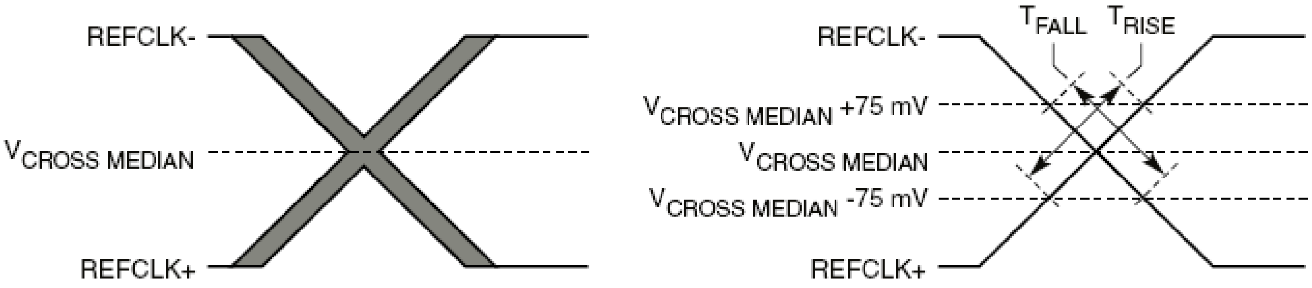


Figure 9. Single-Ended Measurement Points for Rise and Fall Time Matching

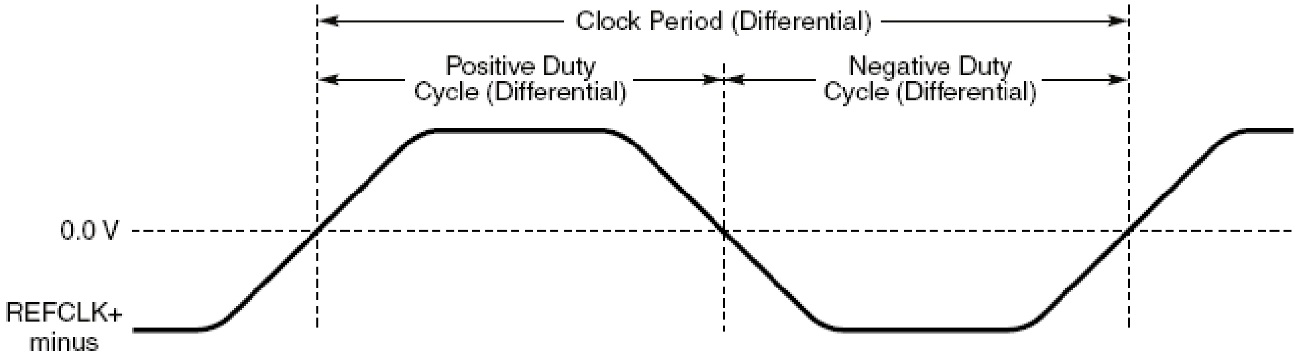


Figure 10. Differential Measurement Points for Duty Cycle and Period

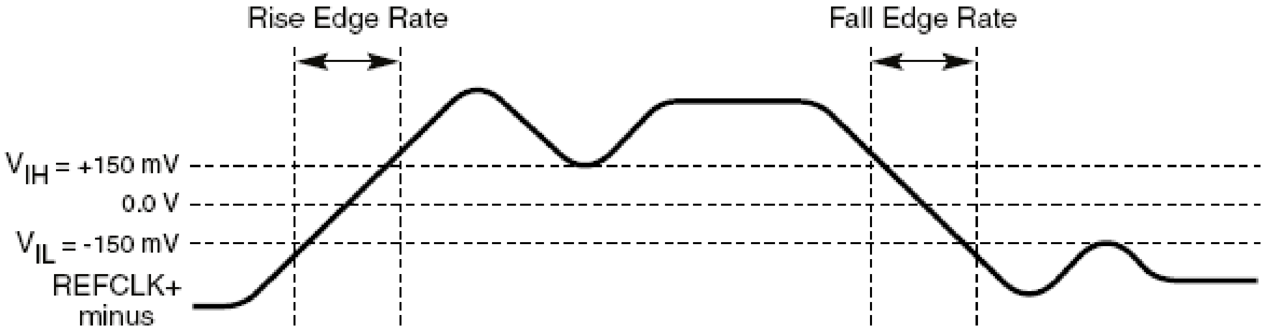


Figure 11. Differential Measurement Points for Rise and Fall Time

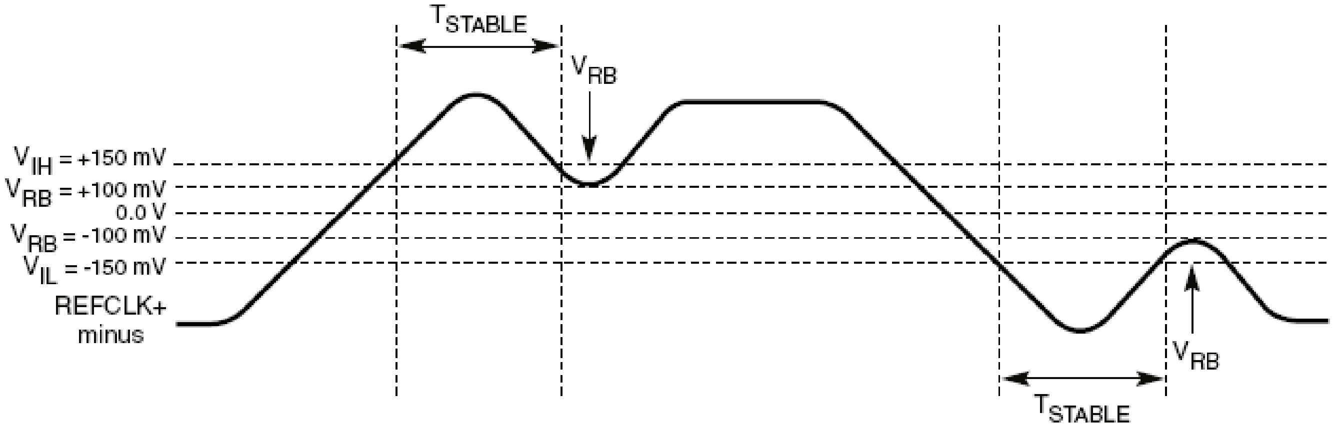


Figure 12. Differential Measurement Points for Ringback

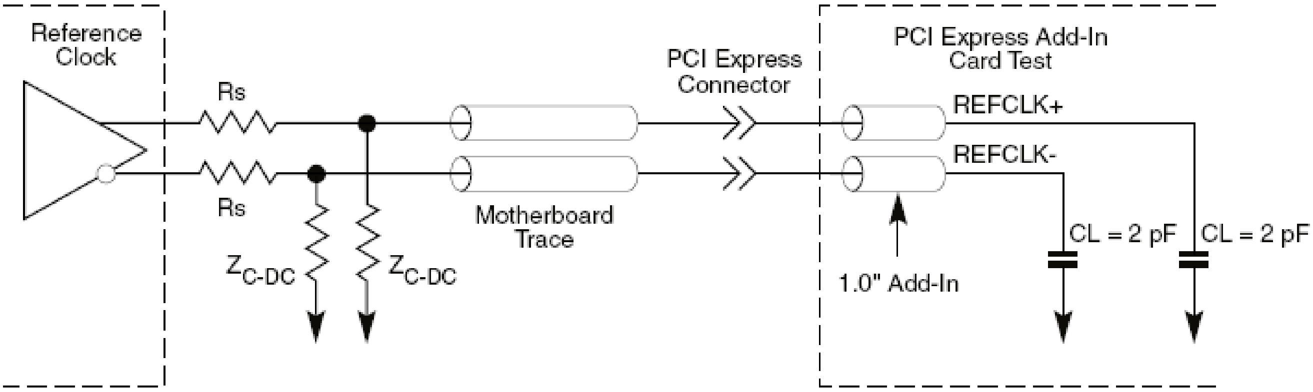


Figure 13. Reference Clock System Measurement Point and Loading

11.4.4. Auxiliary Signal Timing Parameters

Table 33. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK Stable before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
T_{FAIL}	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{WKRF}	LANWAKEB Rise/Fall Time	-	100	ns

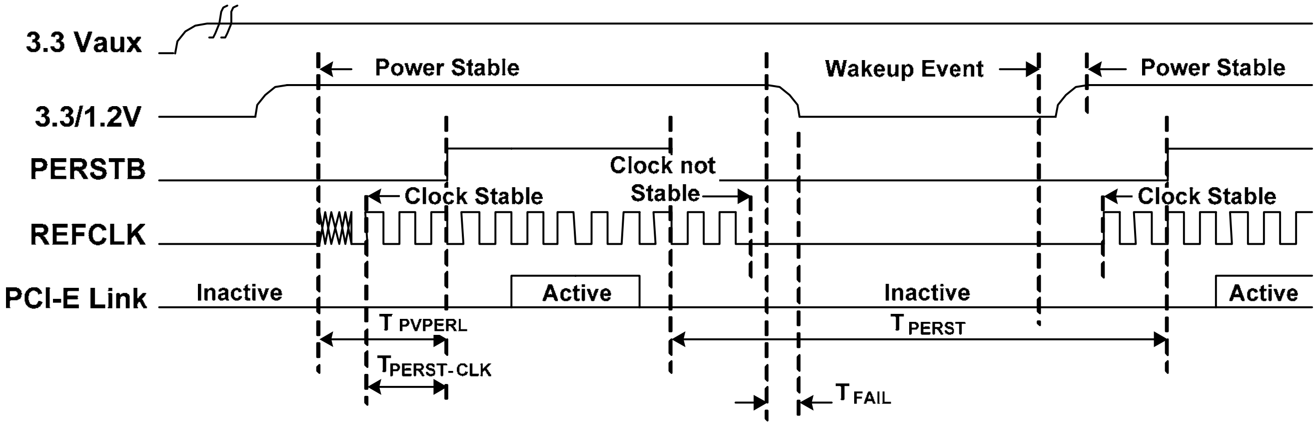
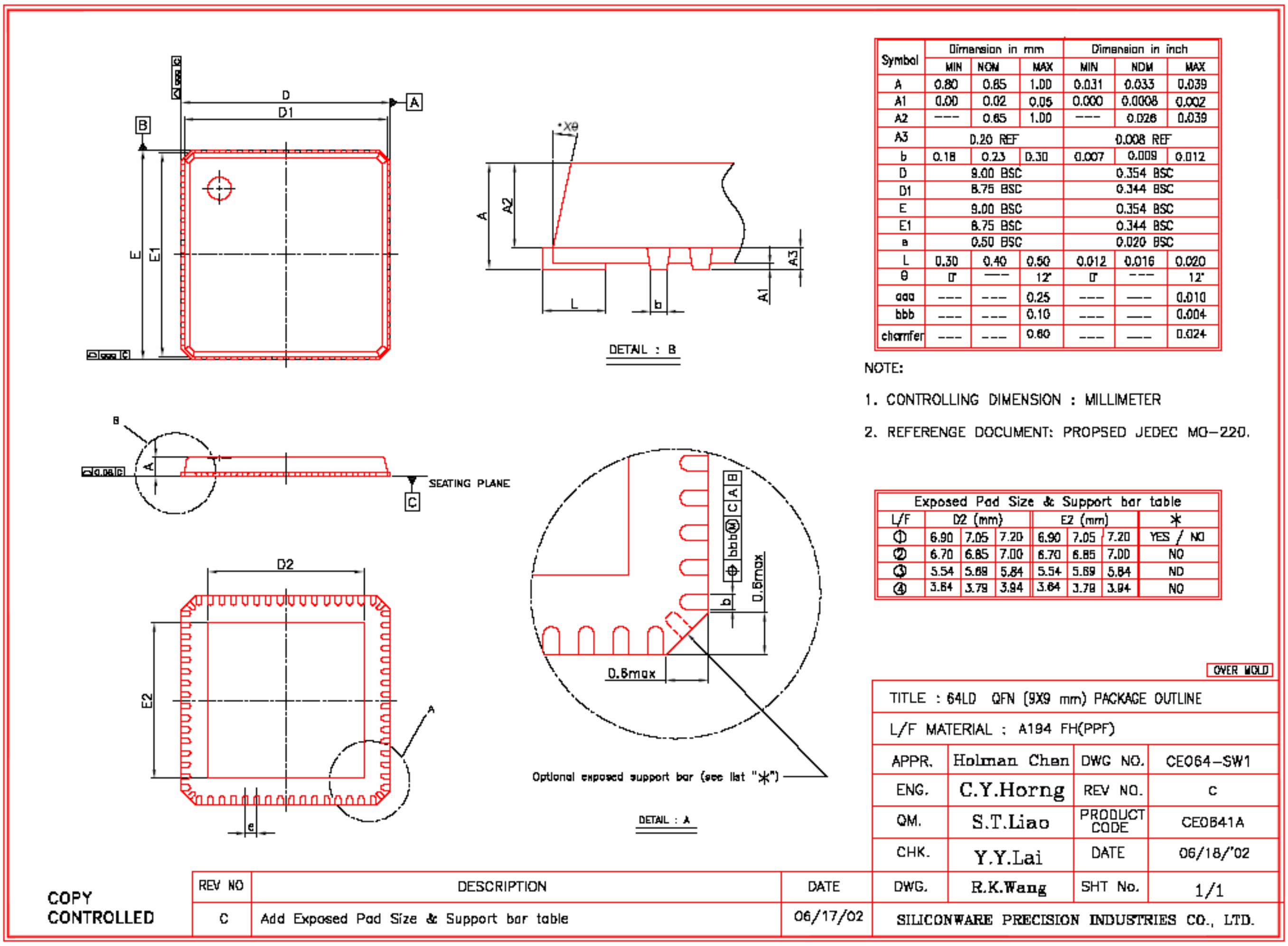


Figure 14. Auxiliary Signal Timing

12. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	0.20 REF			0.008 REF		
b	0.18	0.23	0.30	0.007	0.009	0.012
D	9.00 BSC			0.354 BSC		
D1	8.75 BSC			0.344 BSC		
E	9.00 BSC			0.354 BSC		
E1	8.75 BSC			0.344 BSC		
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
chamfer	---	---	0.60	---	---	0.024

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENGE DOCUMENT: PROPSED JEDEC MO-220.

Exposed Pad Size & Support bar table

L/F	D2 (mm)			E2 (mm)			*
①	6.90	7.05	7.20	6.90	7.05	7.20	YES / NO
②	6.70	6.85	7.00	6.70	6.85	7.00	NO
③	5.54	5.69	5.84	5.54	5.69	5.84	NO
④	3.64	3.79	3.94	3.64	3.79	3.94	NO

TITLE : 64LD QFN (9X9 mm) PACKAGE OUTLINE

L/F MATERIAL : A194 FH(PPF)

APPR.	Holman Chen	DWG NO.	CE064-SW1
ENG.	C.Y.Horng	REV NO.	C
QM.	S.T.Liao	PRODUCT CODE	CE0641A
CHK.	Y.Y.Lai	DATE	06/18/'02
DWG.	R.K.Wang	SHT No.	1/1

SILICONWARE PRECISION INDUSTRIES CO., LTD.

REV NO	DESCRIPTION	DATE
C	Add Exposed Pad Size & Support bar table	06/17/02

Note: The RTL8187SE Exposed Pad Size is type 3.

13. Ordering Information

Table 34. Ordering Information

Part Number	Package	Status
RTL8187SE-GR	64-Pin E-pad QFN with Green Package	Production

Note: See page 7 for Green package identification.

Realtek Semiconductor Corp.
HeadqµArters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com.tw